

C19-A SLI ver1.0

Rev: 1.0

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1.0	1.0	44		11/28/05

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Crush19

PCB : 244 x 244 mm ; 4 layers

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	E/F/G/H	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4
EPCI1	22	A/B/C/D	PREQ-5	PGNT-5
EPCI2	23	B/C/D/A	PREQ-5	PGNT-5

INTEL
P4 Processor
PSC, Smithfield -
LGA 775 pin

PCIEx8 SOLT2 SLI PCIEx8 SOLT1

PCIEx1 SOLT1
PCIEx1 SOLT2

nVIDIA
Crush 19
1040pin FC-BGA

DDIMM1: DDR2 Socket 240P
DDIMM2 : DDR2 Socket 240P
DDIMM3: DDR2 Socket 240P
DDIMM4 : DDR2 Socket 240P

Analog Display
RAMDAC: 400MHz
Resolutions Up To 2048x1536@75Hz

BW : 2GB/s (Support Lsoch)

USB V2.0
USB1 2 ports USB2 2 ports USB3 2 ports USB4 2 ports

nVIDIA
MCP51

BW : 133MB/s @Freq : 33MHz
PCI1 Slot 120pin
PCI2 Slot 120pin
PCI3 Slot 120pin

Up to Ultra ATA/100
One IDE Channel
IDE2 40pin IDE1 40pin

Line in
Line out
Mic in
Center/Bass out
Surround
Side-Surround

Audio Codec
ALC880


SATA1 7Pin
SATA2 7pin
SATA3 7Pin
SATA4 7pin
BW : 150MB/s

intel
FWH
32pin PLCC

TPM 1.1

Super I/O
ITE8712F
128pin PQFP

VIA 1394 (OPTION)
CONN/HEADER
RTL8100C 10/100 Lan
USBLAN RJ45
Marvell GIGA Lan
USBLAN RJ45

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Title

System Block Diagram

Size B

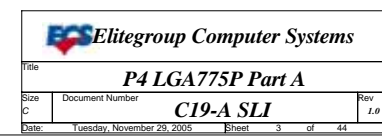
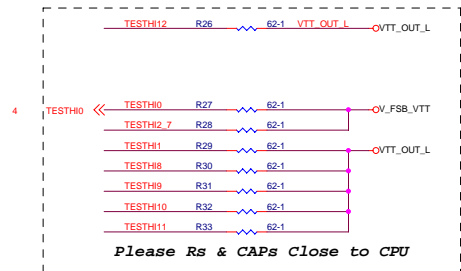
Document Number

C19-A SLI

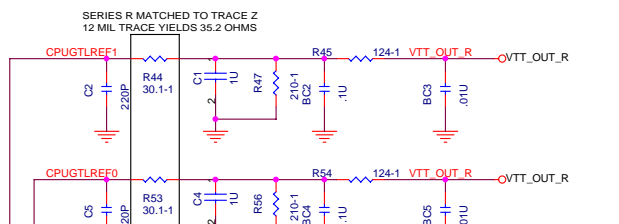
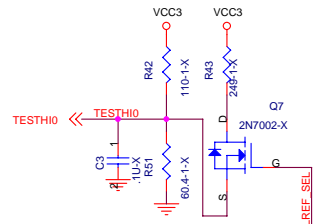
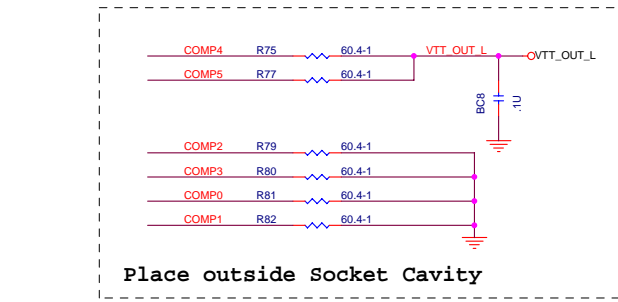
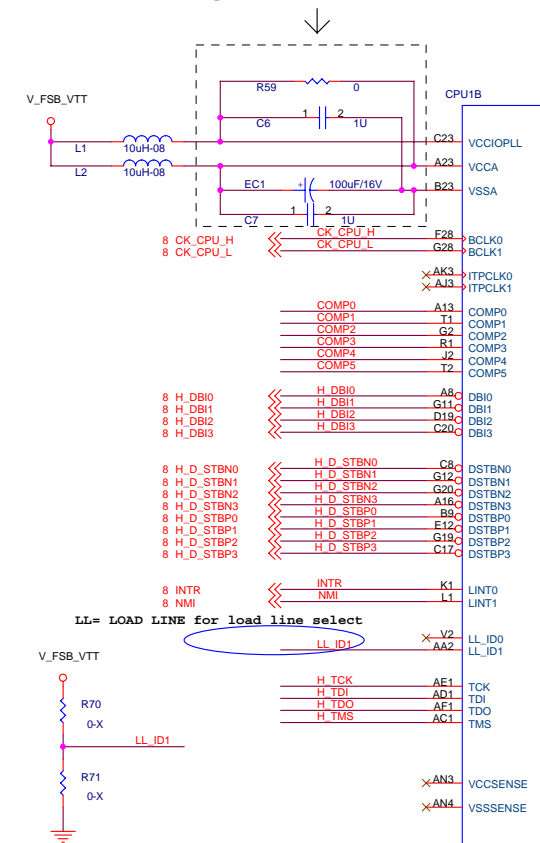
Date: Tuesday, November 29, 2005

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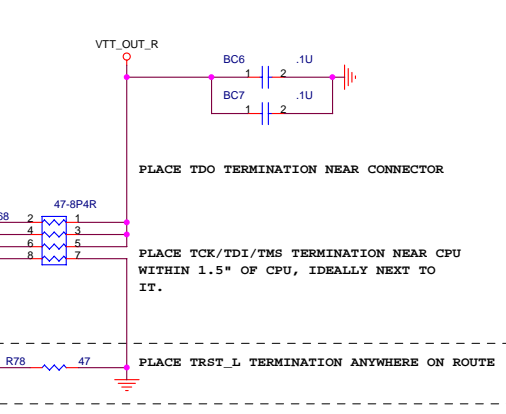
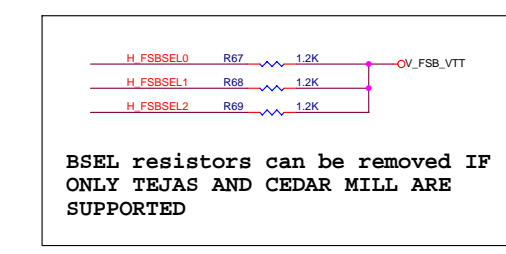
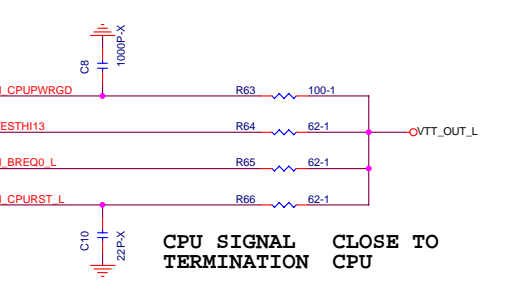
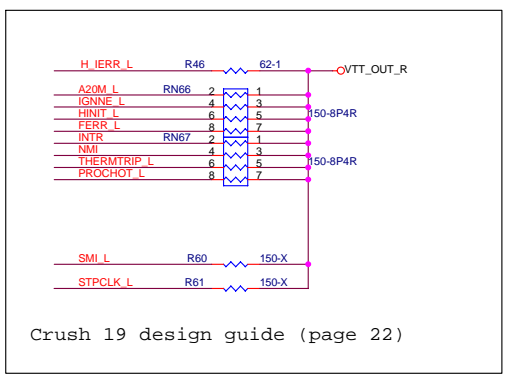
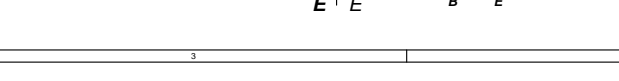
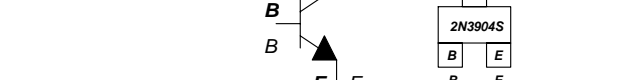
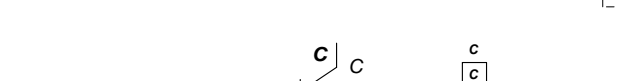
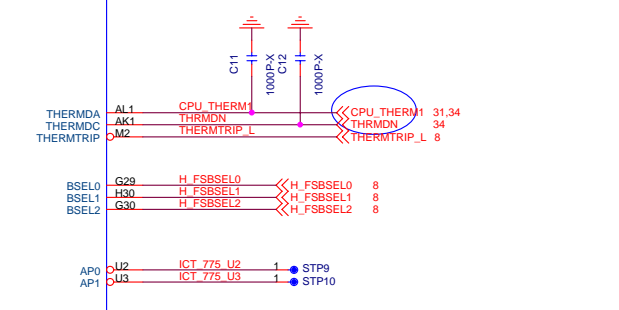


Place componets as close as possible to Processor socket
trace width to cap must be no smaller than 12 Mils



GTLREF= 0.67 * VTT = 0.8V
GTLREF GENERATION CIRCUITS

A20M	K3	A20M_L	<<A20M_L	8
ADS	C2	H_ADS_L	<<H_ADS_L	8
ADSTB0	R6	H_A_STB0	<<H_A_STB0	8
ADSTB1	AD5	H_A_STB1	<<H_A_STB1	8
BINIT	AD3	H_BNR_L	<<H_BNR_L	8
BNR	C2	H_BPRI_L	<<H_BPRI_L	8
BPR	C8	H_BREQ0_L	<<H_BREQ0_L	8
BRO	E3	H_BREQ1_L	<<H_BREQ1_L	8
DBR	AC2	HWRST_L	<<HWRST_L	26.44
DBSY	B2	H_DBSY_L	<<H_DBSY_L	8
DEFER	C1	H_DRDY_L	<<H_DRDY_L	8
DRDY	C7	H_DRDY_L	<<H_DRDY_L	8
EDRDY	F2	CPU_FC5	<<CPU_FC5	8
FERR/PBE	R3	FERR_L	<<FERR_L	8
HIT	D4	H_HIT_L	<<H_HIT_L	8
HITM	E4	H_HITM_L	<<H_HITM_L	8
IERR	AB2	H_IERR_L	<<H_IERR_L	8
IGNNE	N2	IGNNE_L	<<IGNNE_L	8
INIT	C3	H_LOCK_L	<<H_LOCK_L	8
LOCK	AB3	H_LOCK_L	<<H_LOCK_L	8
MCERR	G5	CPU_FC7	<<CPU_FC7	8
PC_REC	AL2	PROCHOT_L	<<PROCHOT_L	8
PROCHOT	N1	H_CPUPWRGD	<<H_CPUPWRGD	8
PWRGOOD	G23	H_CPURST_L	<<H_CPURST_L	8
RESET	H4	TESTH13	<<TESTH13	8
RSP	L2	SMI_L	<<SMI_L	8
SLP	P2	STPCLK_L	<<STPCLK_L	8
STPCLK	M3	H_TRDY_L	<<H_TRDY_L	8
TRDY	E3	H_TRDY_L	<<H_TRDY_L	8
TRST	AG1	H_TRST_L	<<H_TRST_L	8



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File: **P4 LGA775P Part B**

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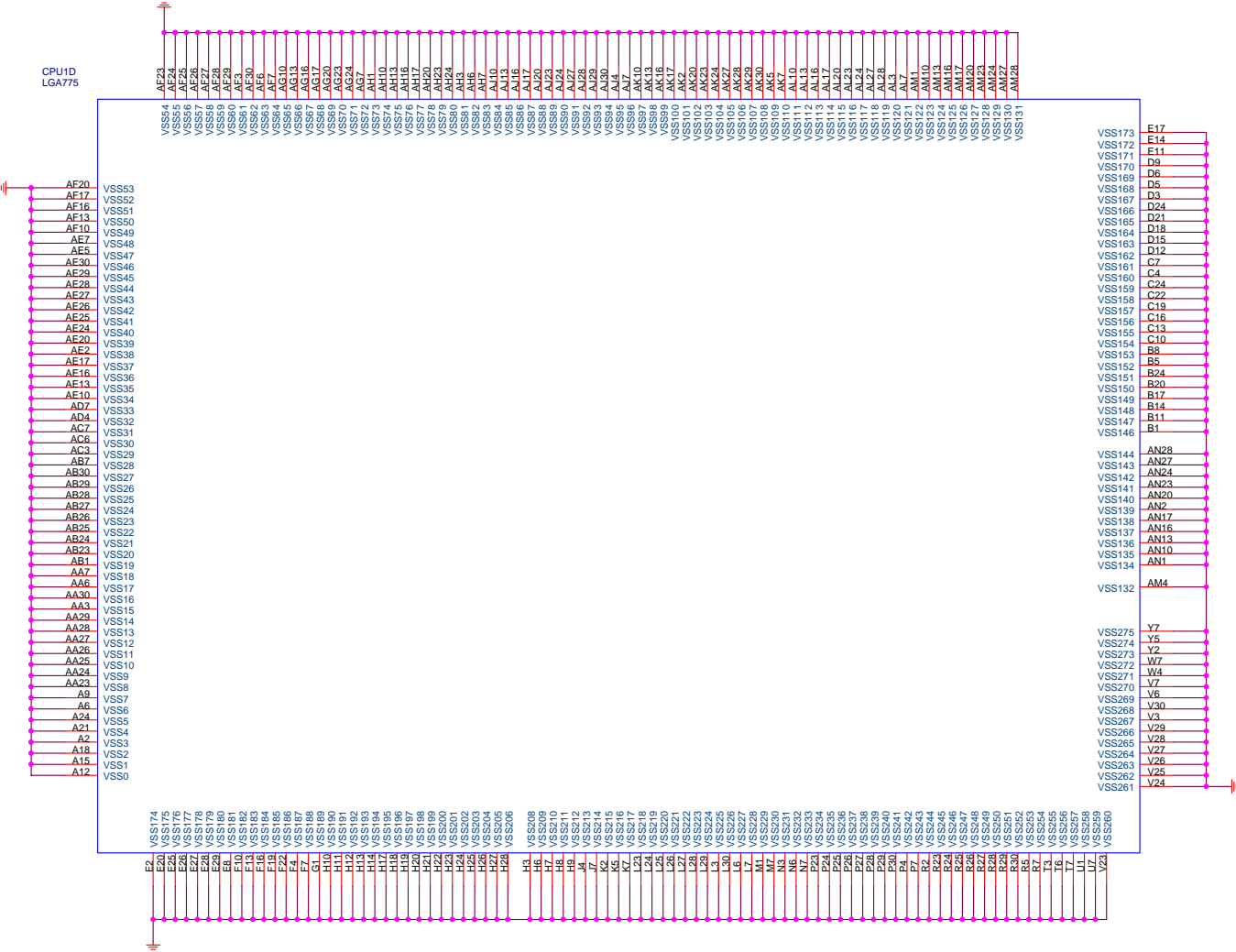
CPU1C
LGA775



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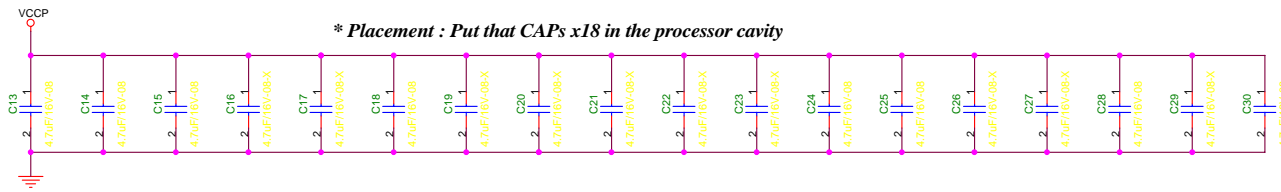
Title			P4 LGA775P Part C
Size	Document Number	Rev	
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CPU1D
LGA775



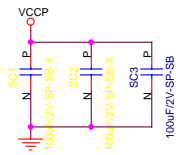
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Title			P4 LGA775P Part D		
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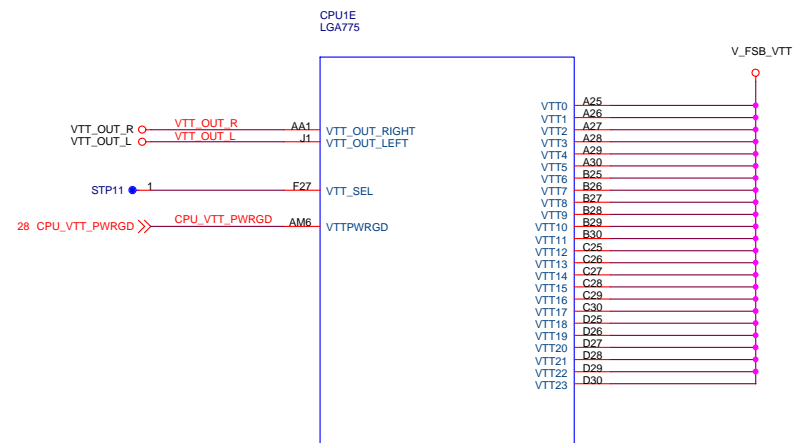


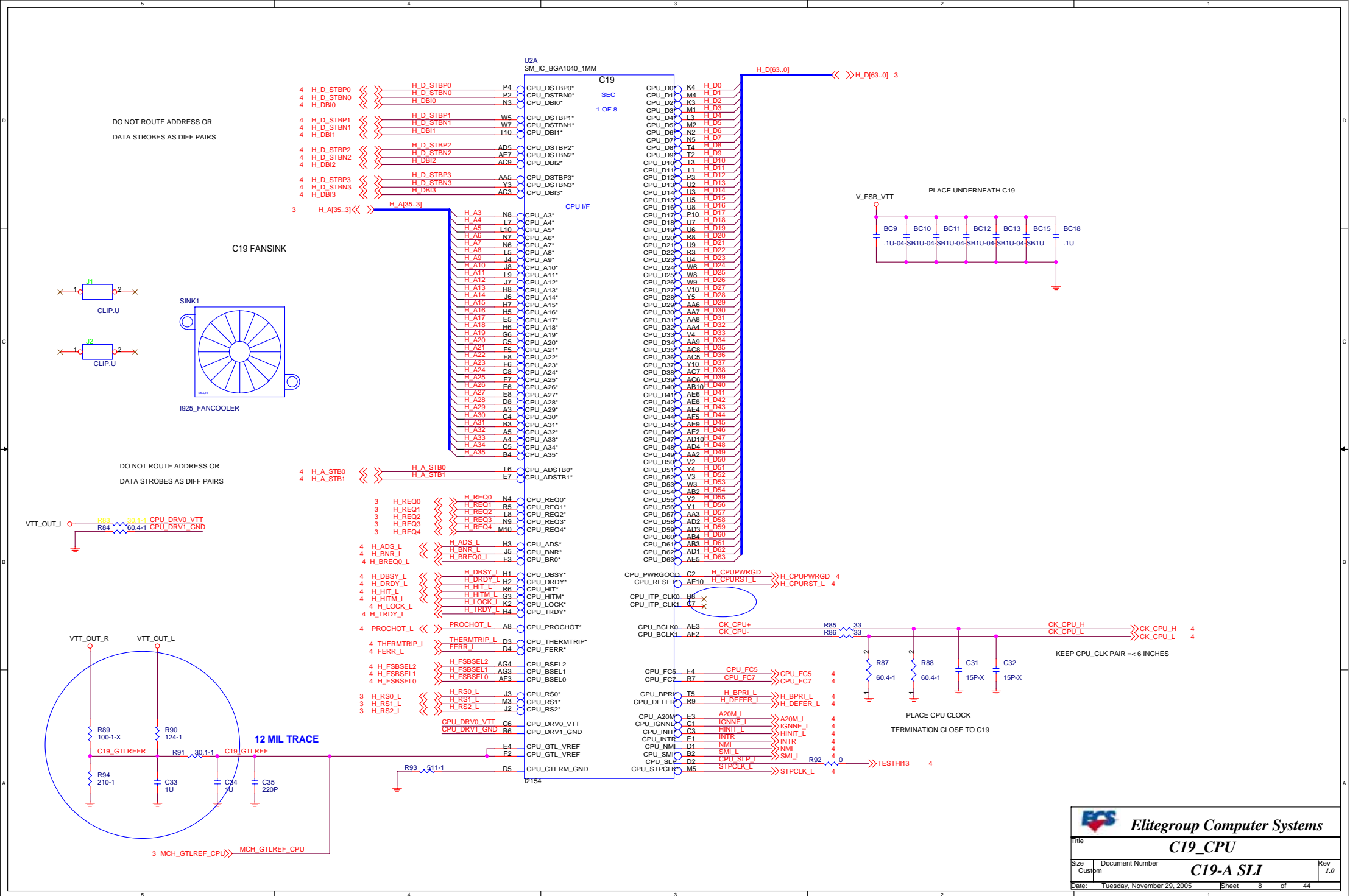
** Placement : Put that CAPs x18 in the processor cavity*

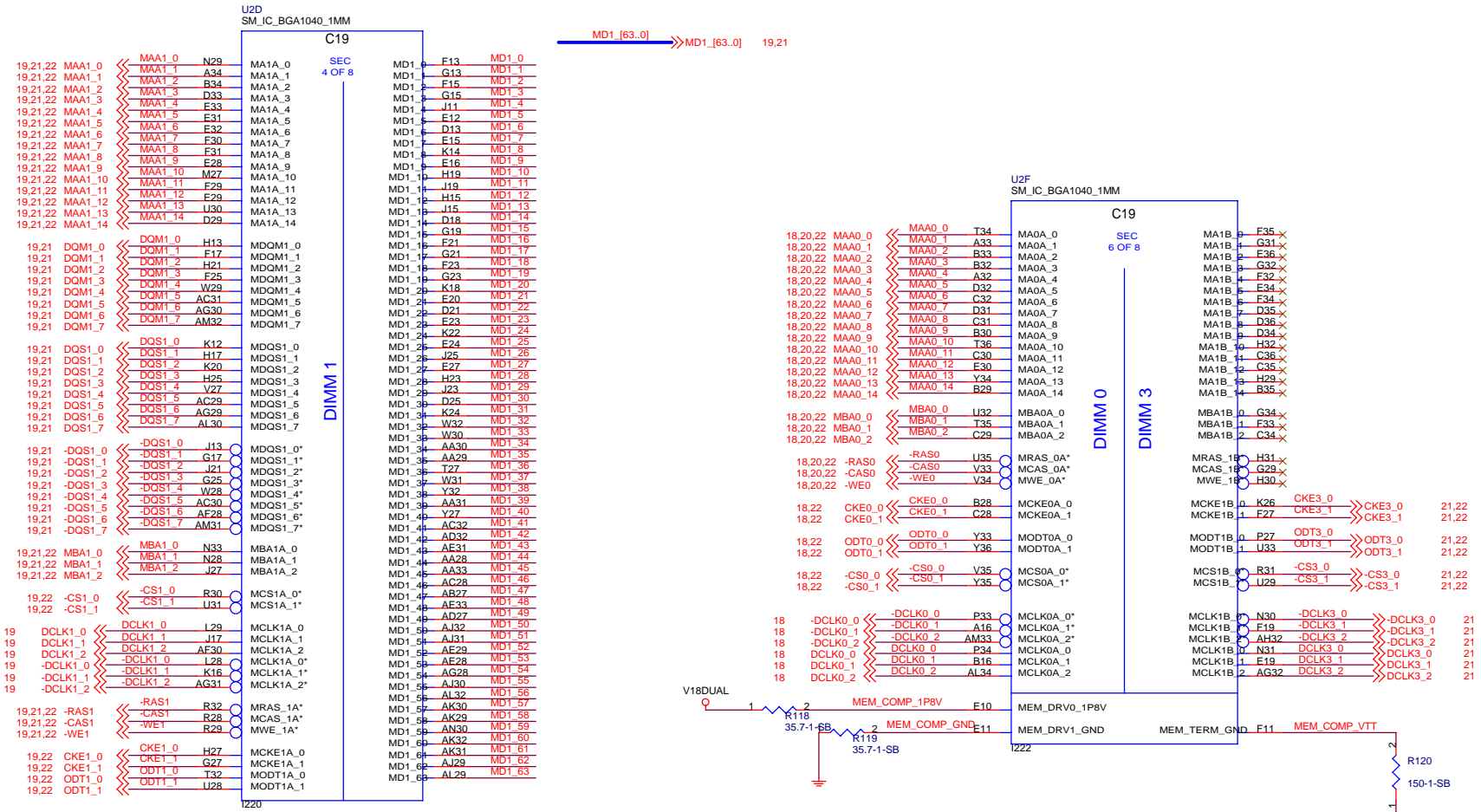
** Placement : Put that CAPs x2 on solder side*

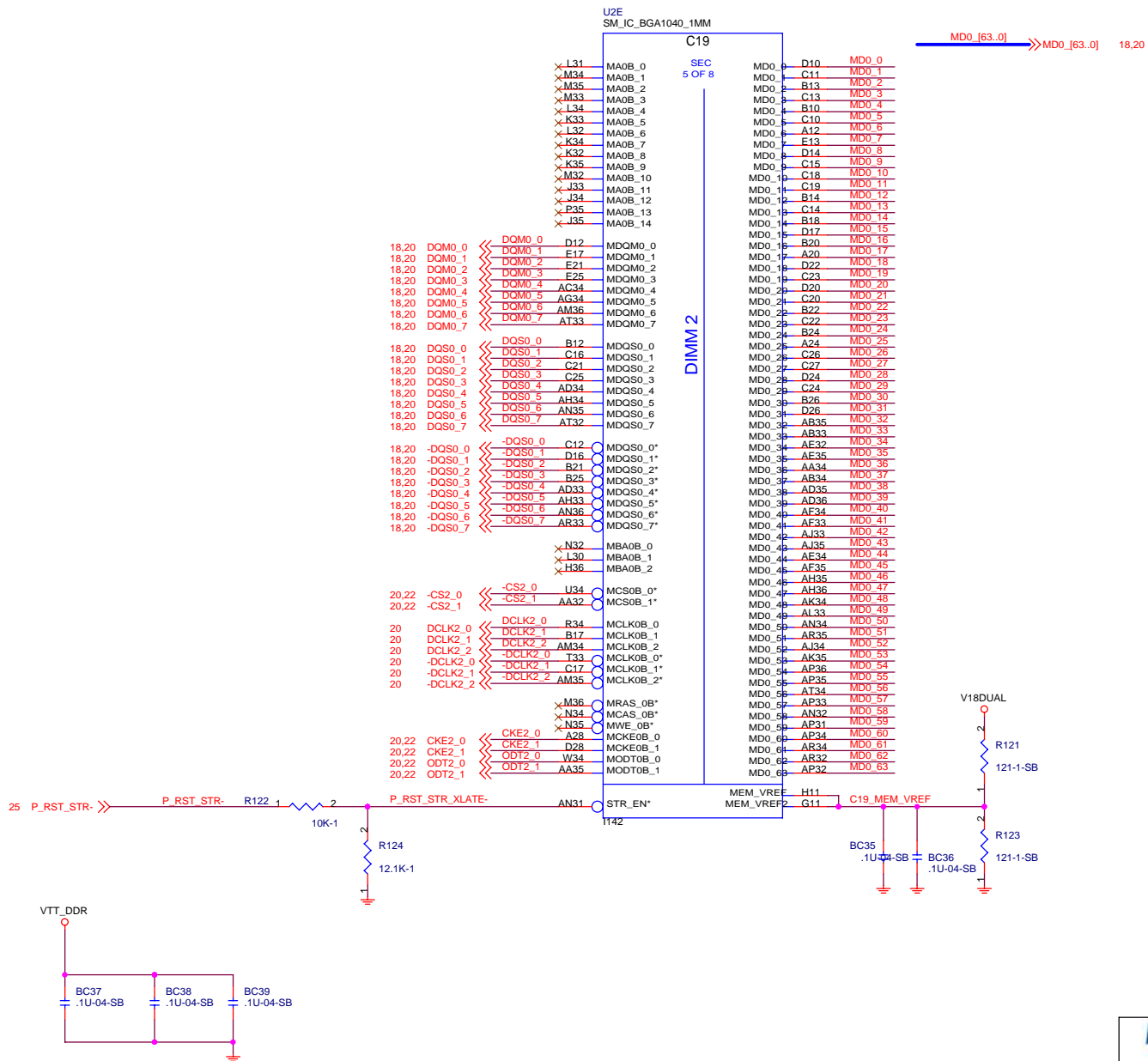


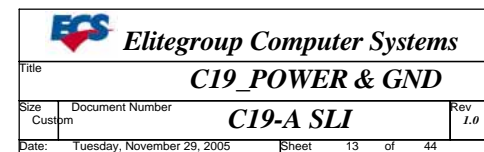
VTT_SEL=0 for the Tejas processor



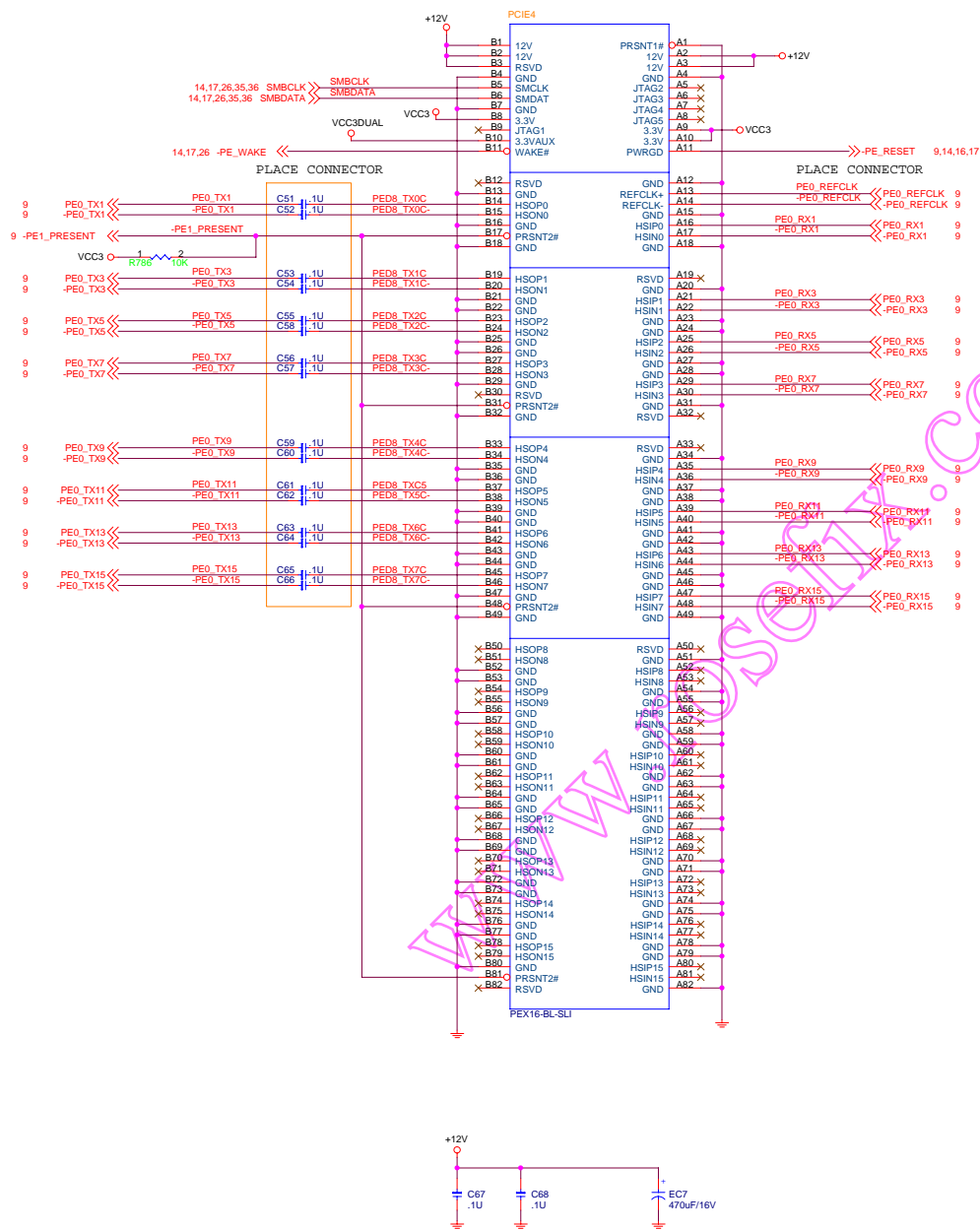


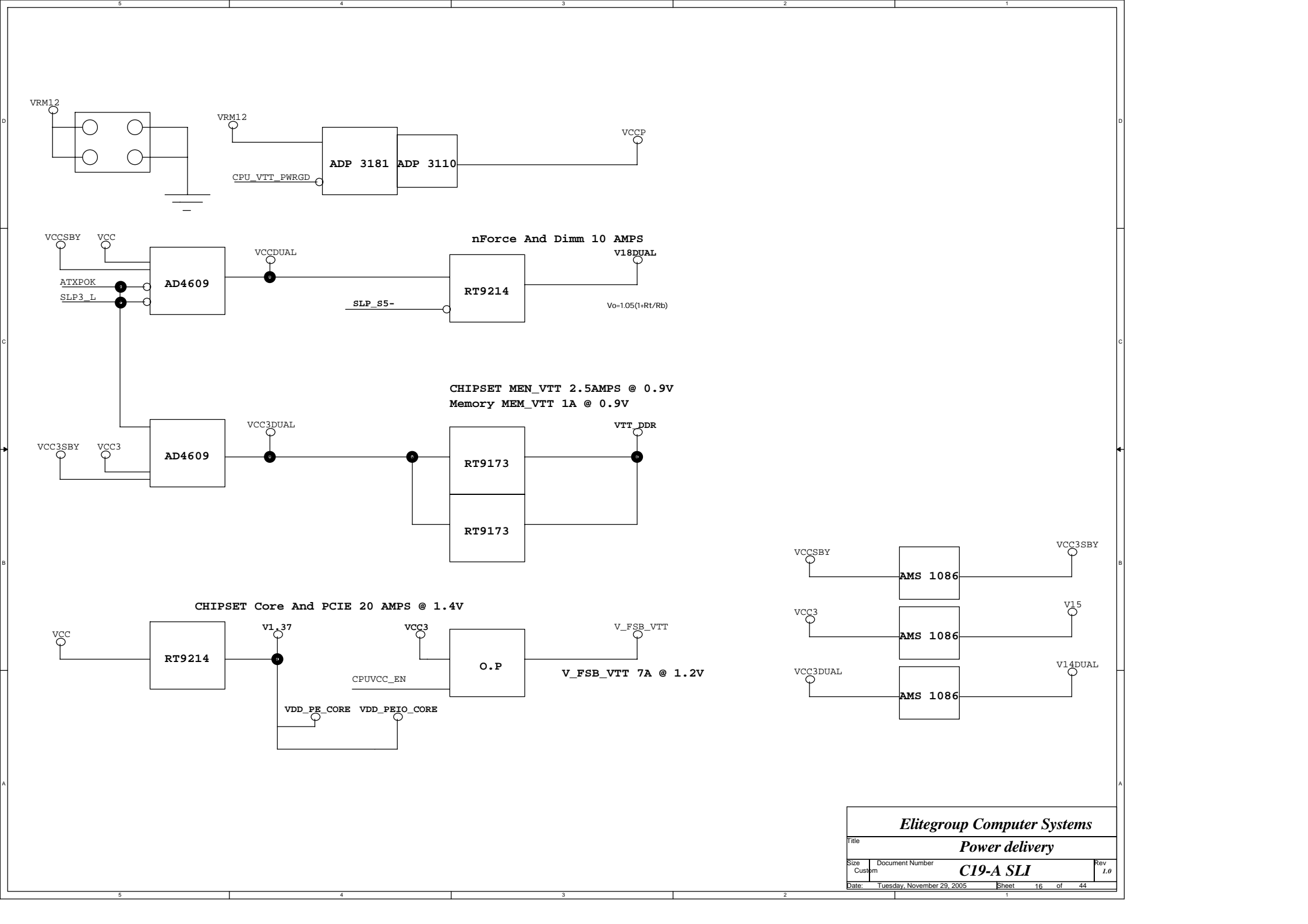


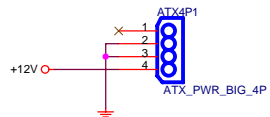
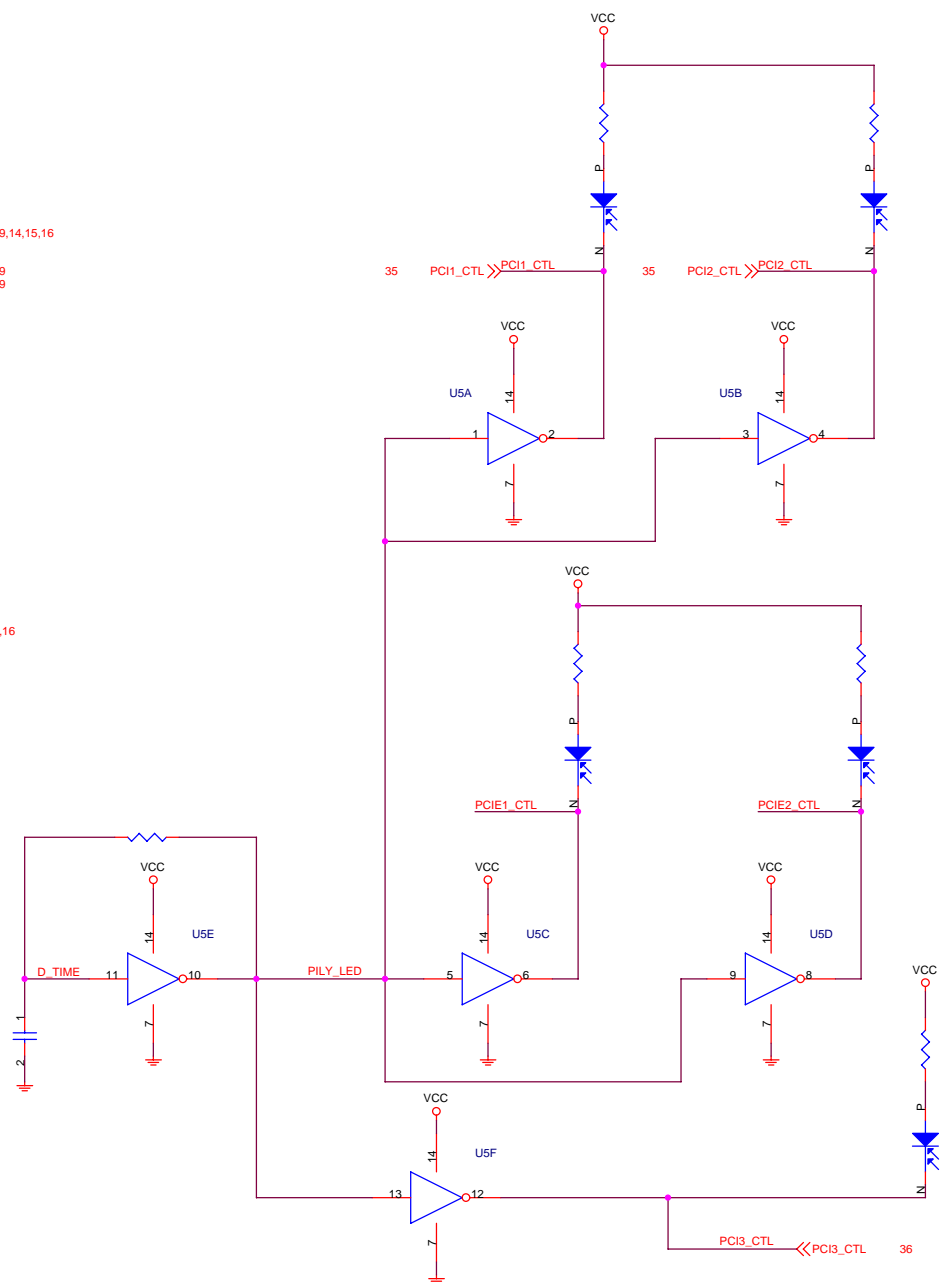




PCI-E *8

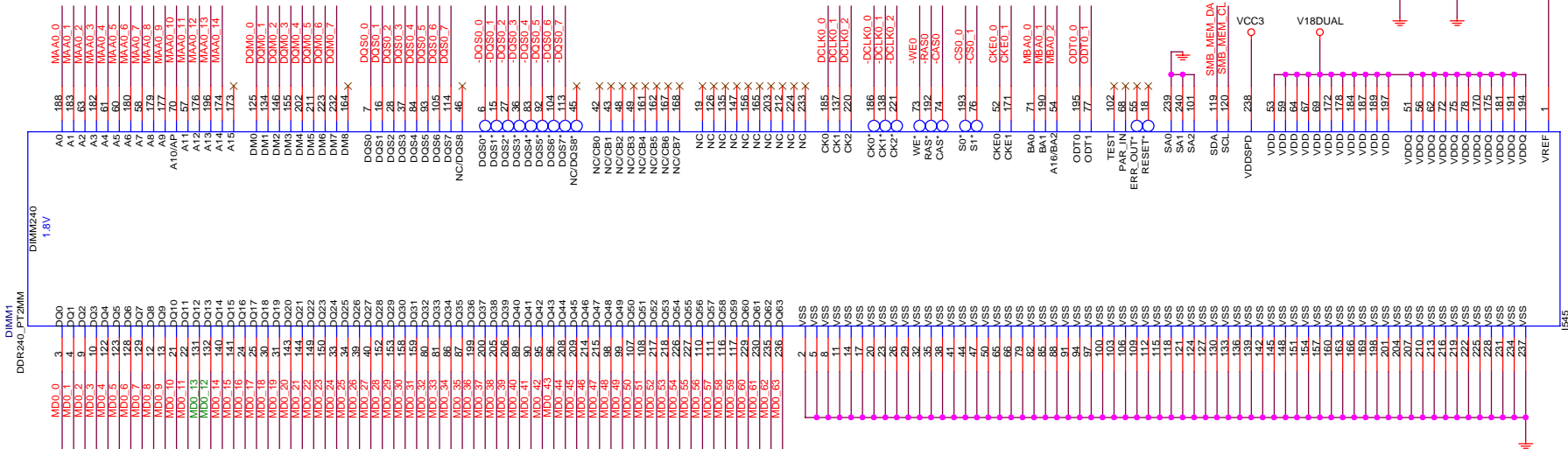
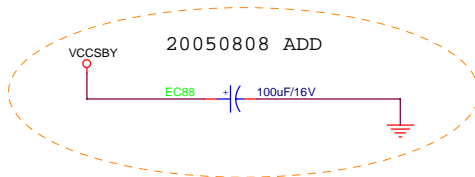
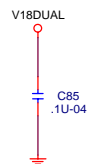
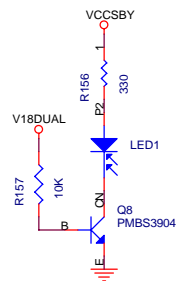
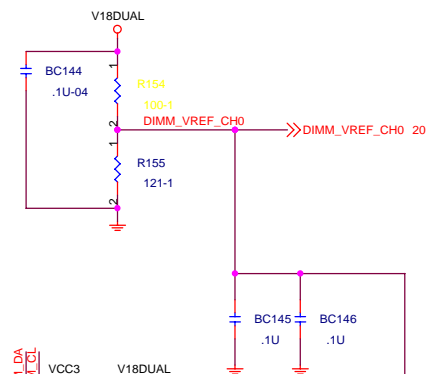
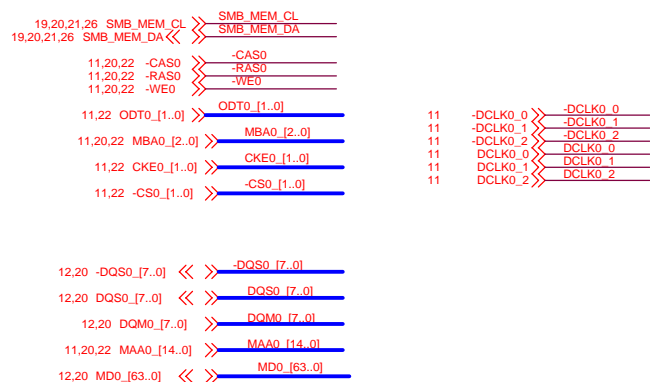
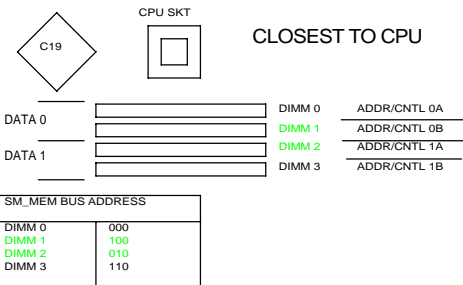






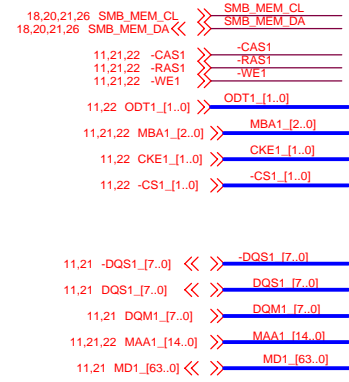
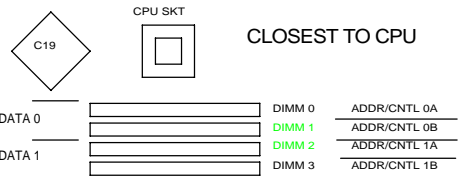
DIMM 0

CHANNEL 0,COPY A

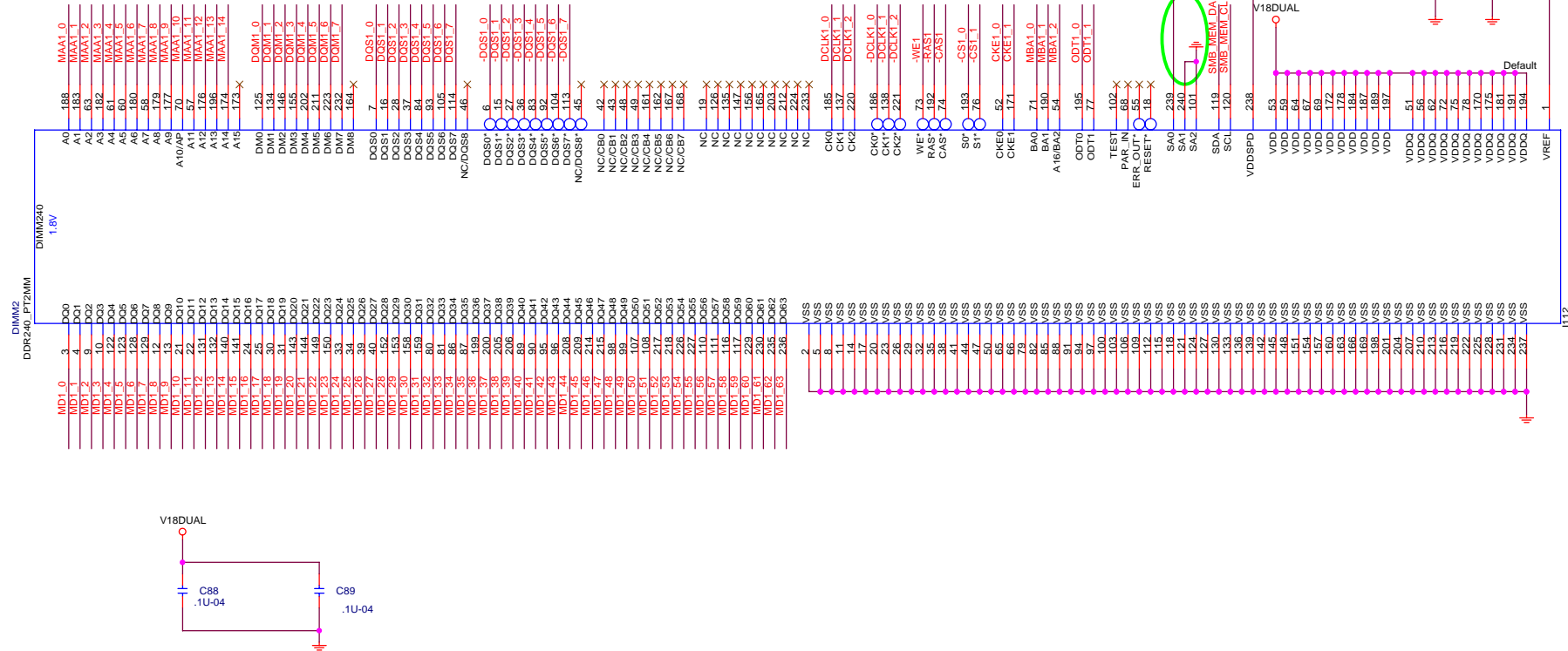



DIMM 1

CHANNEL 1,COPY A



SM_MEM BUS ADDRESS	
DIMM 0	000
DIMM 1	100
DIMM 2	010
DIMM 3	110



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Title

DIMM2

Size

Custpm

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DIMM 2

CHANNEL 0,COPY B



CLOSEST TO CPU

DATA 0

DATA 1

DIMM 0
DIMM 1
DIMM 2
DIMM 3

ADDR/CNTL 0A
ADDR/CNTL 0B
ADDR/CNTL 1A
ADDR/CNTL 1B

SM_MEM BUS ADDRESS

DIMM 0 000
DIMM 1 100
DIMM 2 010
DIMM 3 110

18,19,21,26 SMB_MEM_CL
18,19,21,26 SMB_MEM_DA

11,18,22 -CAS0
11,18,22 -RAS0
11,18,22 -WE0

12,22 ODT2_[1..0]

11,18,22 MBA0_[2..0]

12,22 CKE2_[1..0]

12,22 -CS2_[1..0]

12 DCLK2_0
12 DCLK2_1
12 DCLK2_2
12 -DCLK2_0
12 -DCLK2_1
12 -DCLK2_2

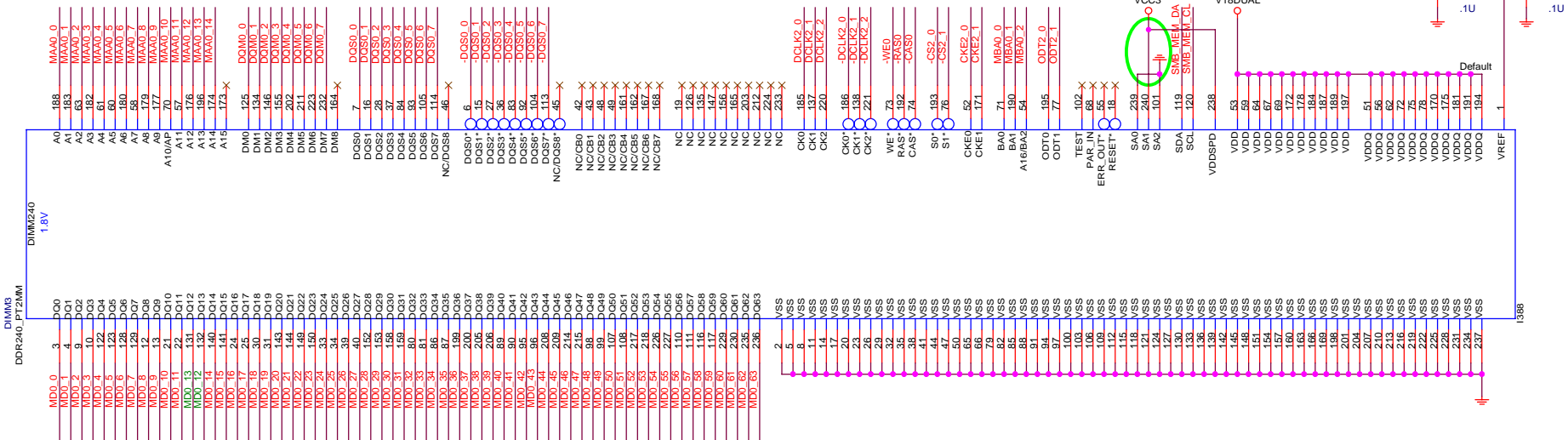
12,18 -DQS0_[7..0]

12,18 DQS0_[7..0]

12,18 DQM0_[7..0]

11,18,22 MAA0_[14..0]

12,18 MD0_[63..0]



DIMM 3

CHANNEL 1,COPY B

FURTHEST FROM CPU

CLOSEST TO CPU



DATA 0

DATA 1

DIMM 0

DIMM 1

DIMM 2

DIMM 3

ADDR/CNTL 0A

ADDR/CNTL 0B

ADDR/CNTL 1A

ADDR/CNTL 1B

SM_MEM BUS ADDRESS

DIMM 0	000
DIMM 1	100
DIMM 2	010
DIMM 3	110

18,19,20,26 SMB_MEM_CL >> SMB MEM CL
18,19,20,26 SMB_MEM_DA << SMB MEM DA

11,19,22 -CAS1 >> -CAS1
11,19,22 -RAS1 >> -RAS1
11,19,22 -WE1 >> -WE1

11,22 ODT3_[1..0] >> ODT3_[1..0]

11,19,22 MBA1_[2..0] >> MBA1_[2..0]

11,22 CKE3_[1..0] >> CKE3_[1..0]

11,22 -CS3_[1..0] >> -CS3_[1..0]

11,19 -DQS1_[7..0] << -DQS1_[7..0]

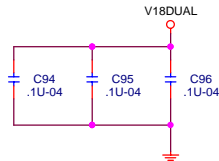
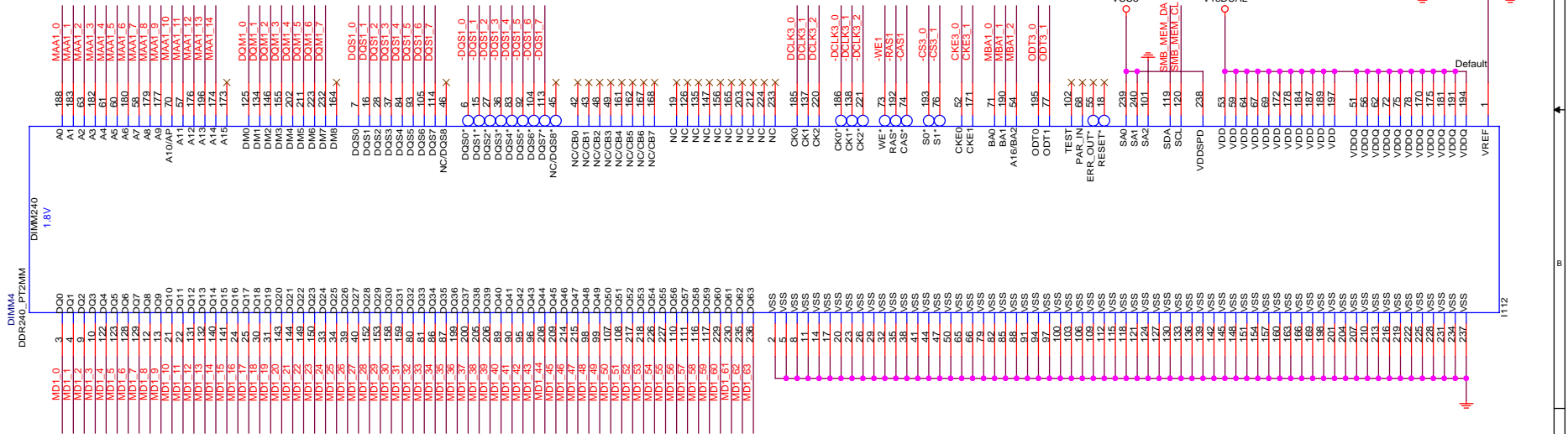
11,19 DQS1_[7..0] << DQS1_[7..0]

11,19 DQM1_[7..0] >> DQM1_[7..0]

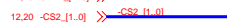
11,19,22 MAA1_[14..0] >> MAA1_[14..0]

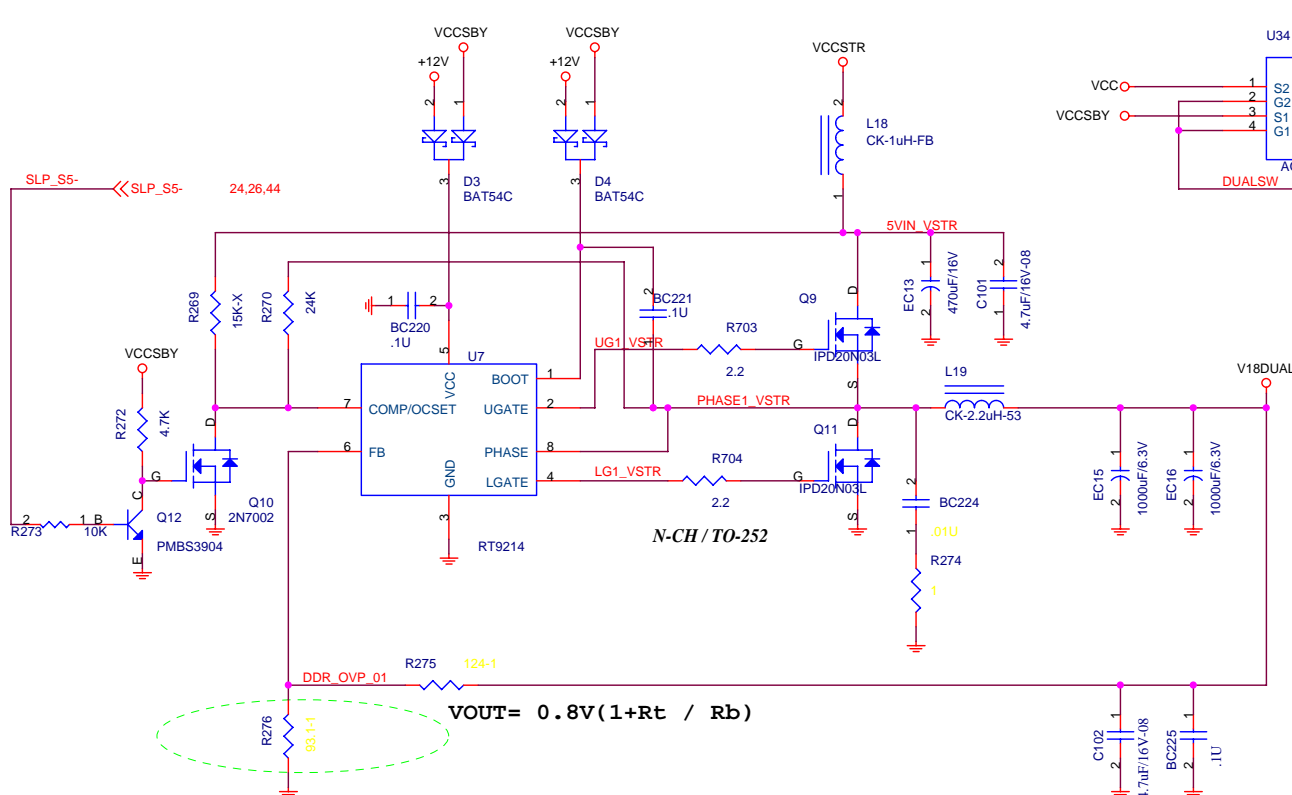
11,19 MD1_[63..0] << MD1_[63..0]

11 -DCLK3_0 >> -DCLK3_0
11 -DCLK3_1 >> -DCLK3_1
11 -DCLK3_2 >> -DCLK3_2
11 DCLK3_0 >> DCLK3_0
11 DCLK3_1 >> DCLK3_1
11 DCLK3_2 >> DCLK3_2



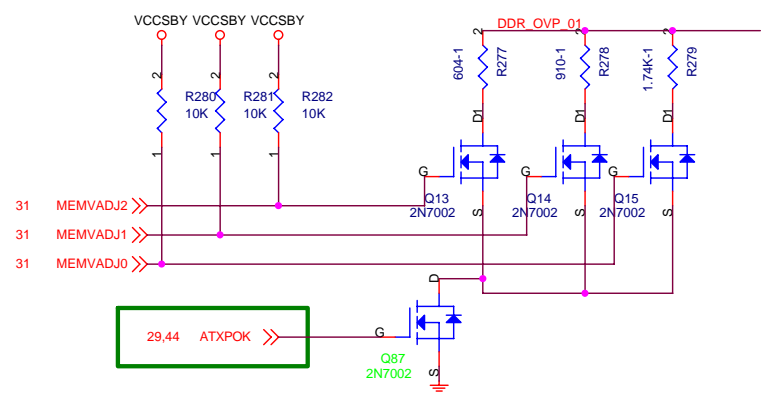
Title		
DIMM4		
Size	Document Number	Rev
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Normal

1_8VSTR should be able to support up to 14A



RT:124-1% RB:93.1-1%

GPIO-10 MJ2	GPIO-55 MJ1	GPIO-53 MJ0	V_DIMM Table	END
0	0	0	1.8V	1.85V
0	0	1	1.85V	1.91V
* 0	1	0	1.9V	1.96V
0	1	1	1.95V	2.02V
* 1	0	0	2.0V	2.02V
1	0	1	2.05V	2.08V
* 1	1	0	2.10V	2.13V
* 1	1	1	2.2V	2.18V

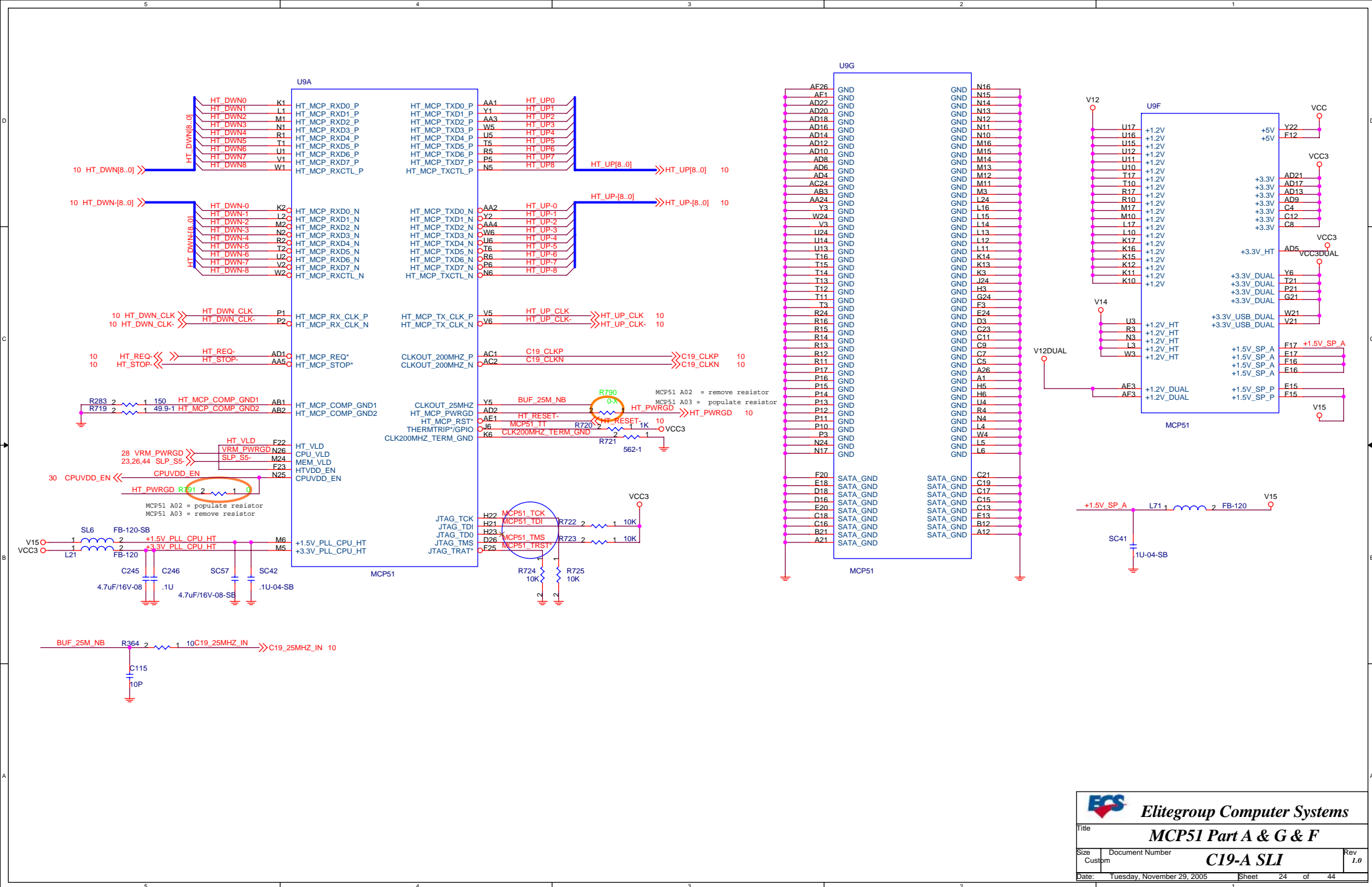
Title: **DDR-II Power**

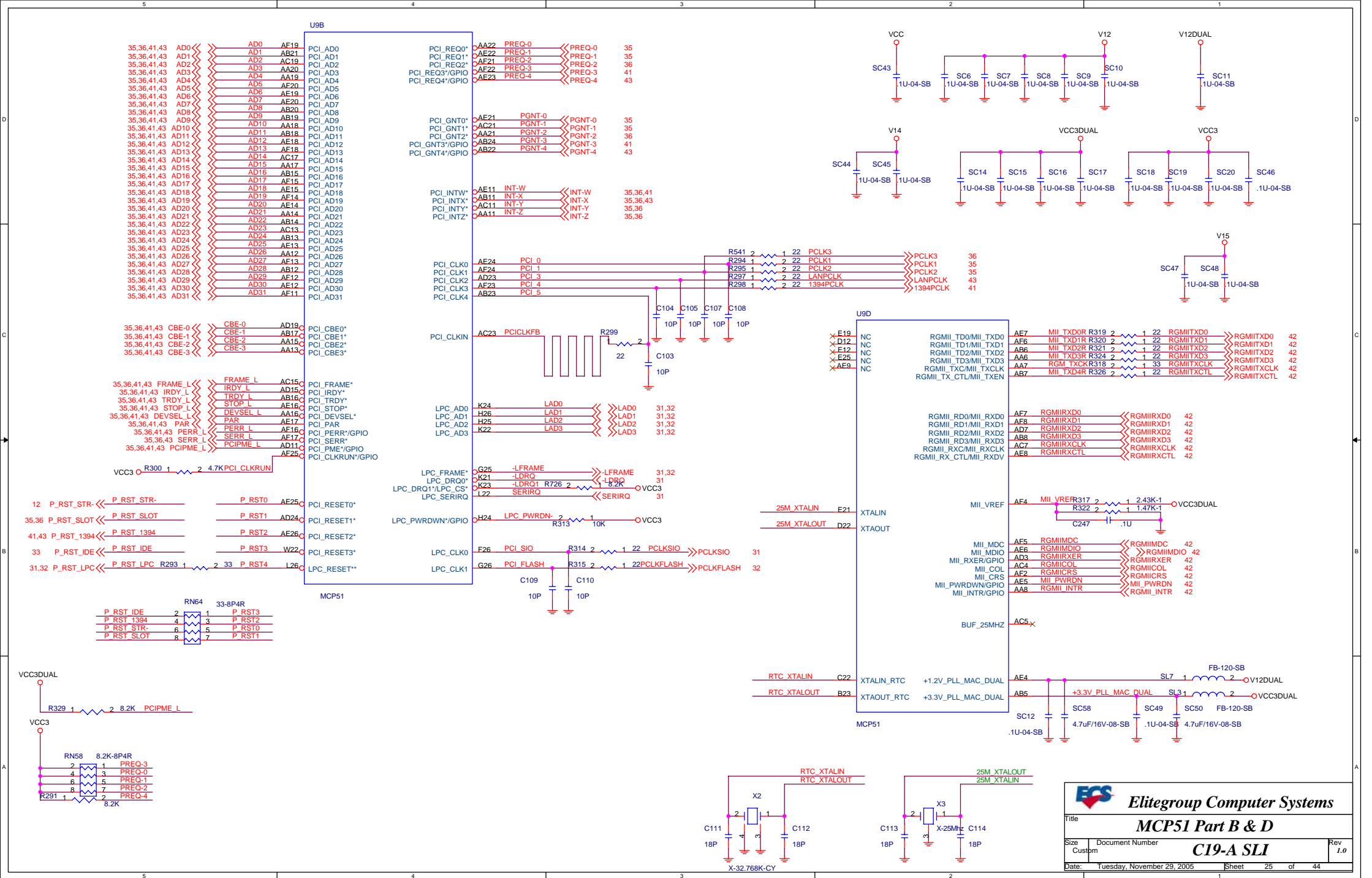
Size: Document Number

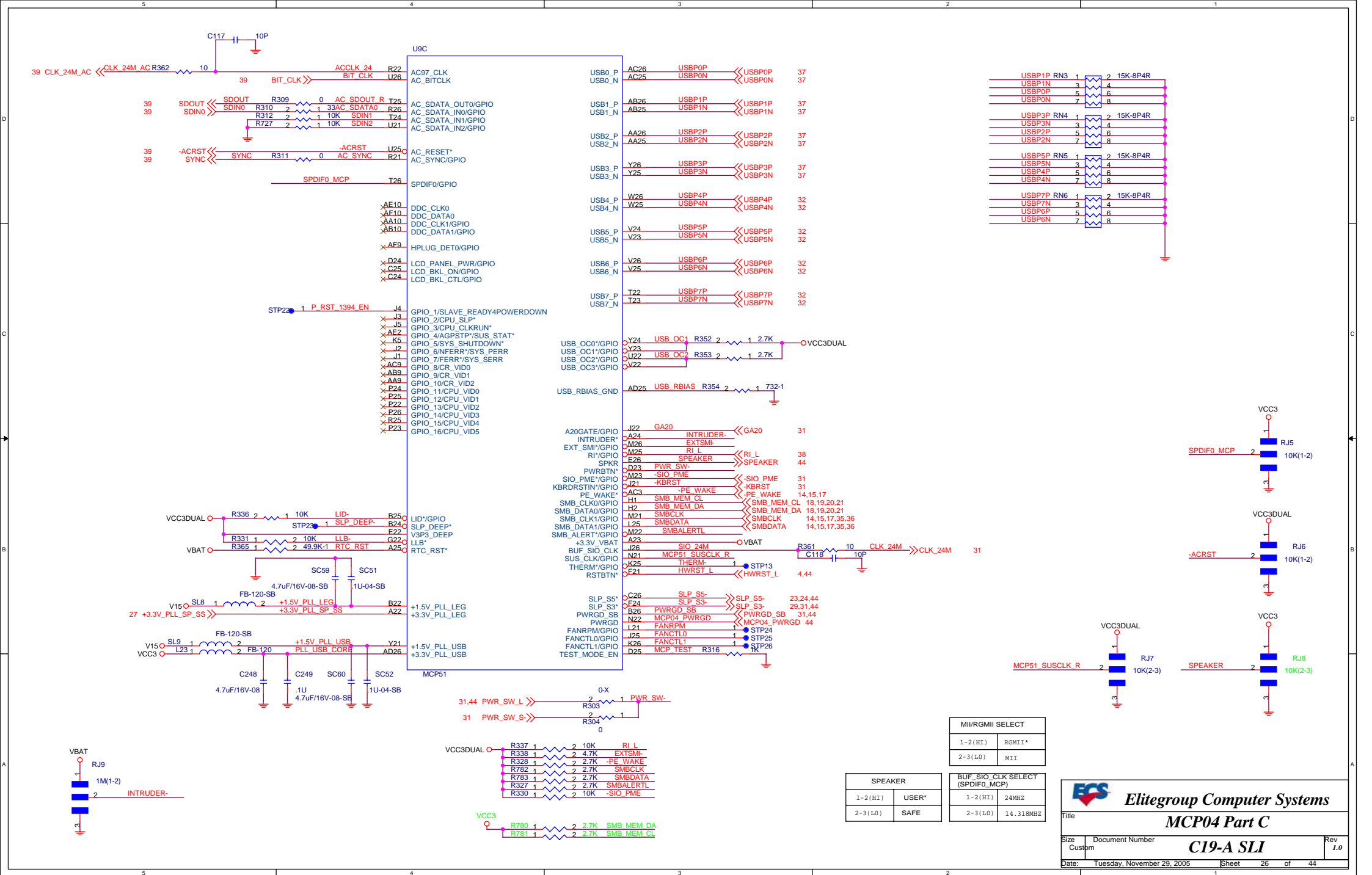
Date: Tuesday, November 29, 2005

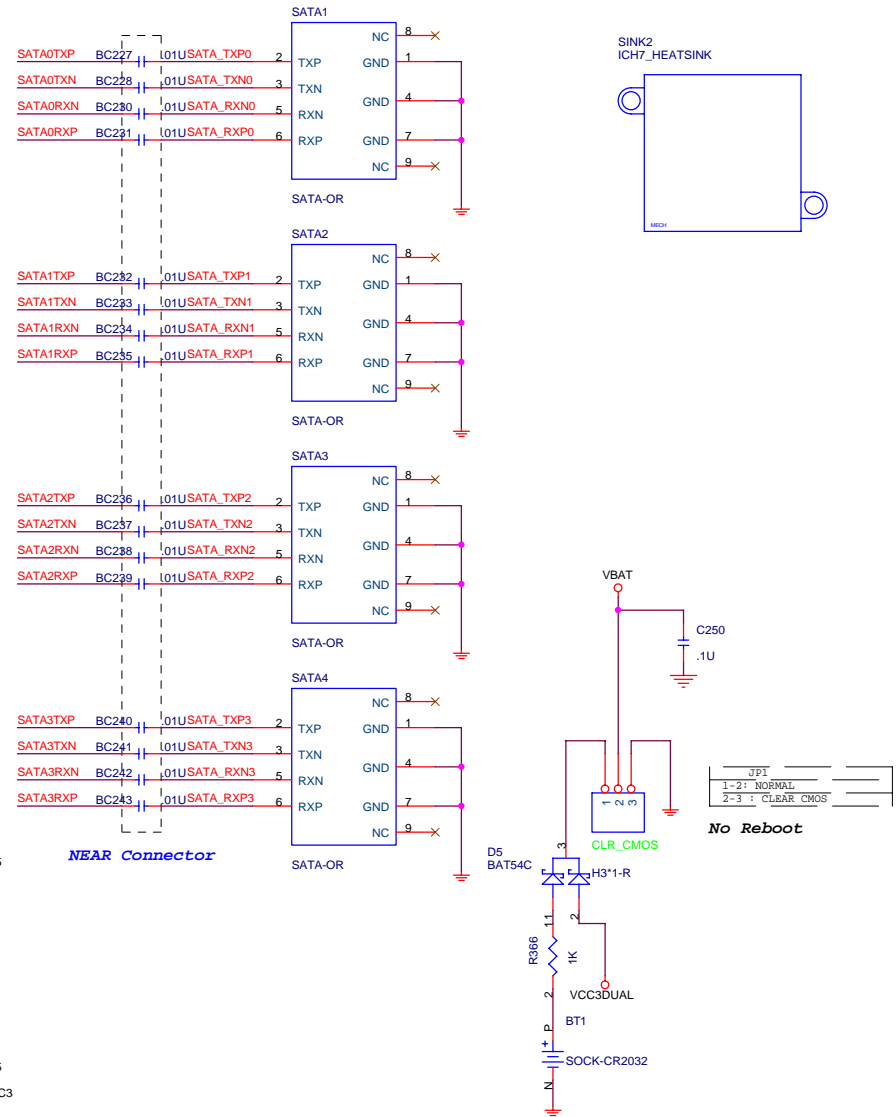
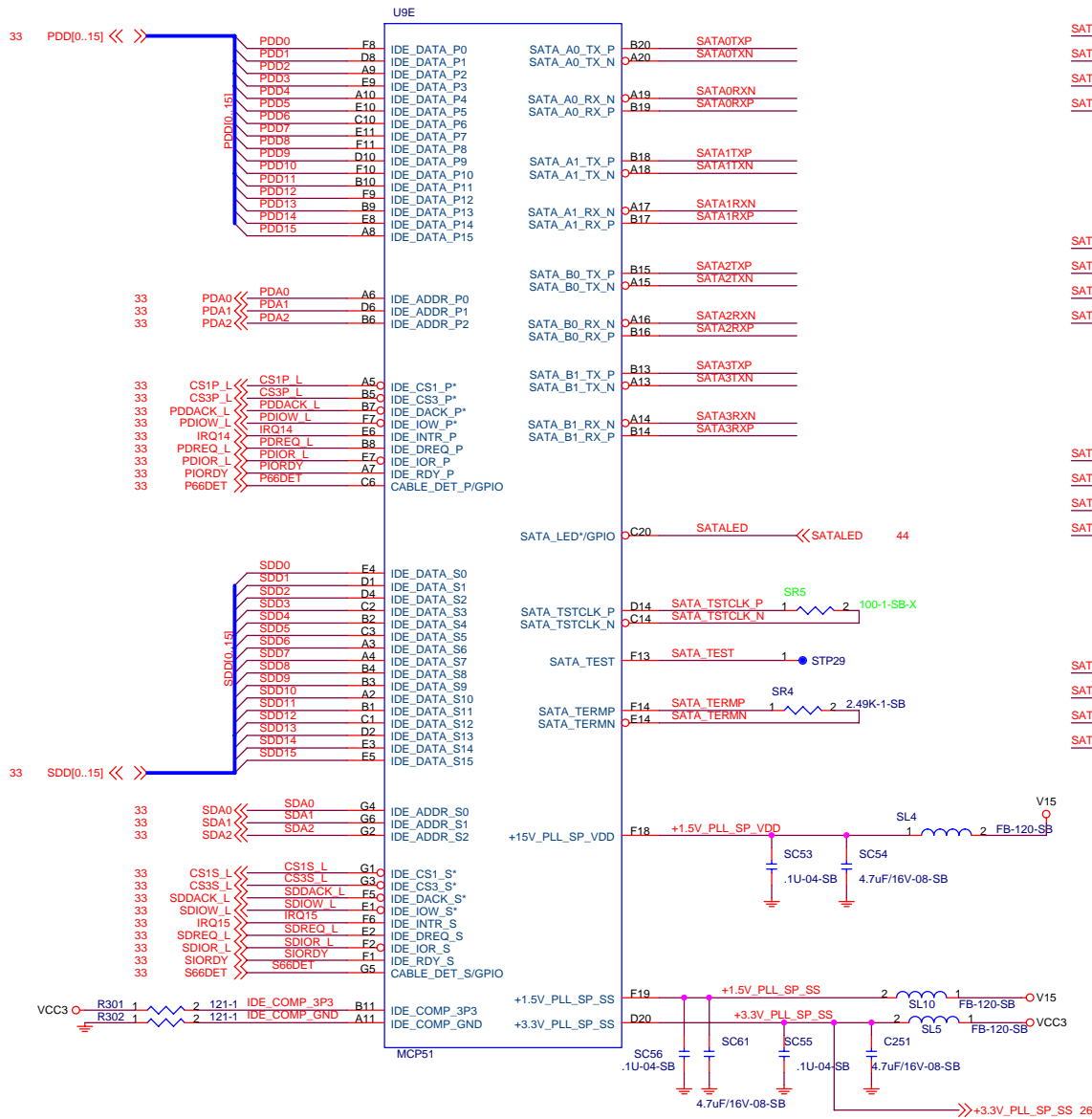
Rev: **1.0**

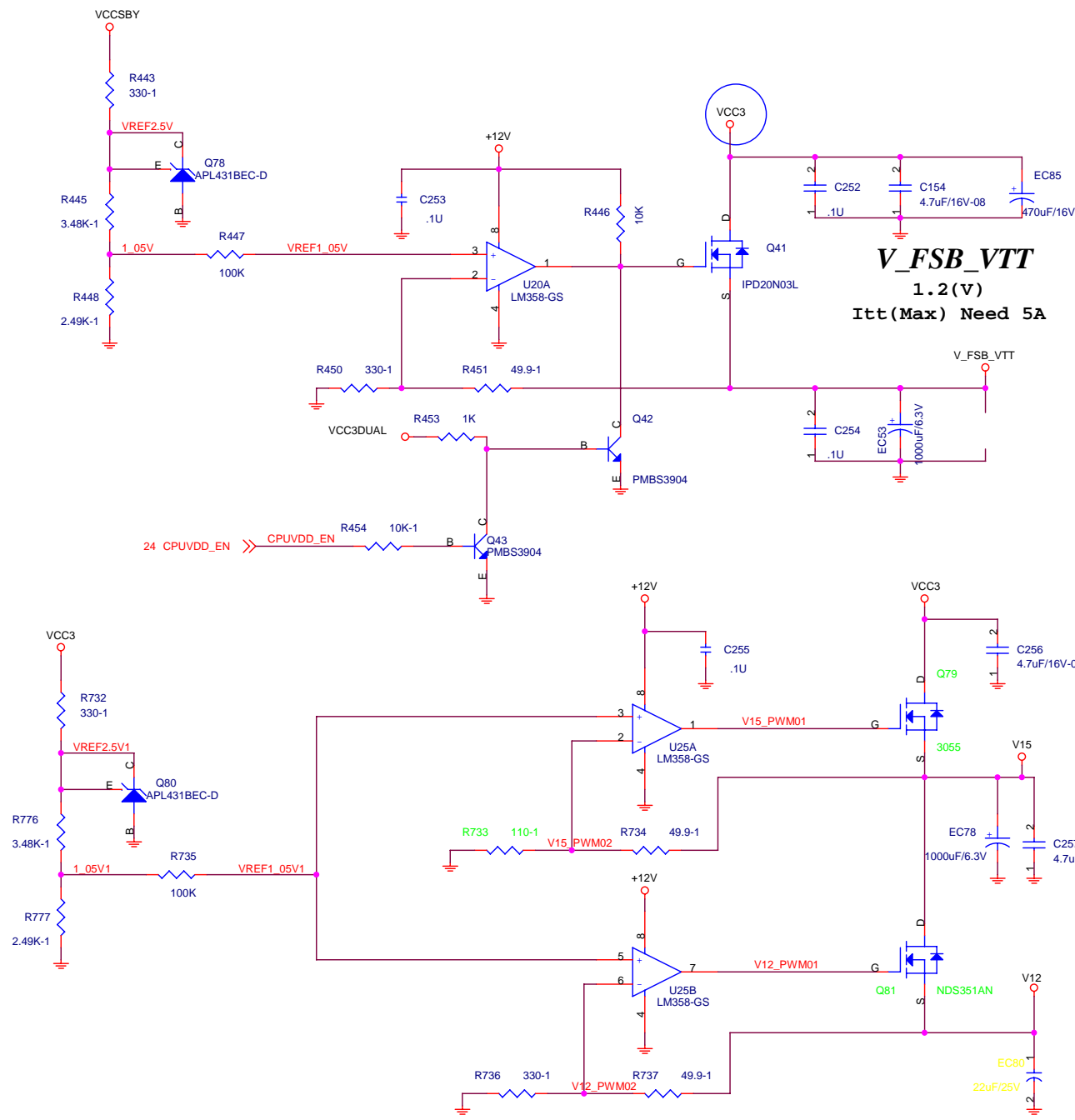
Sheet: 23 of 44



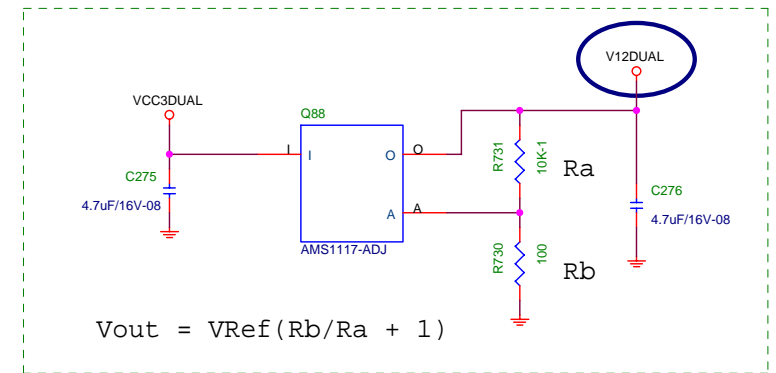


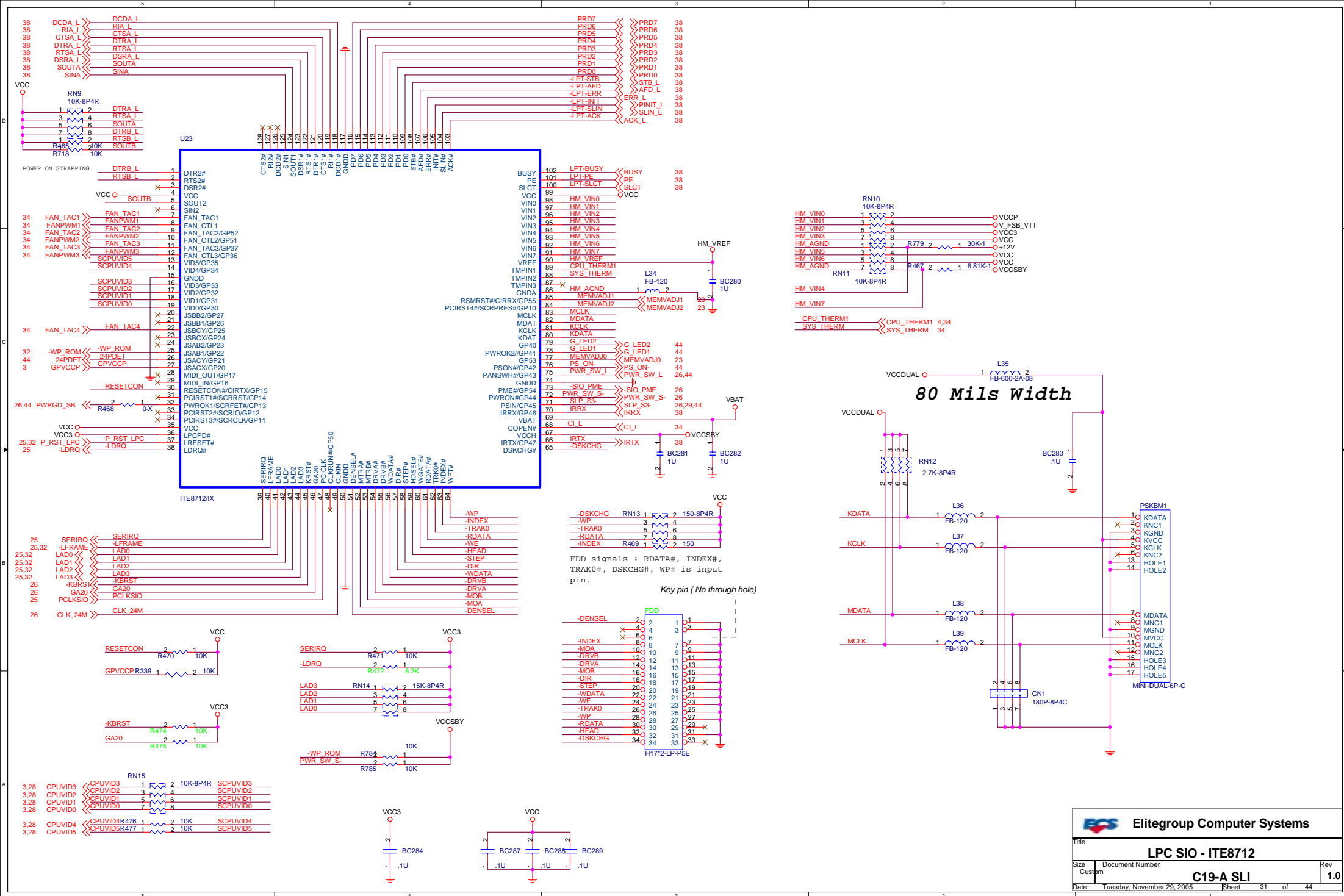




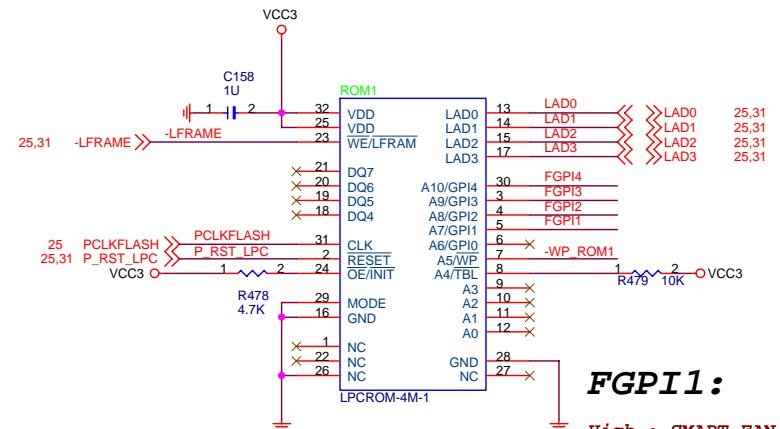
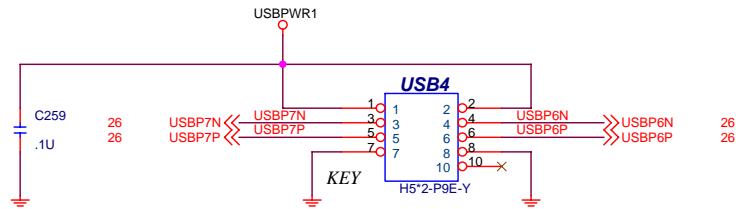
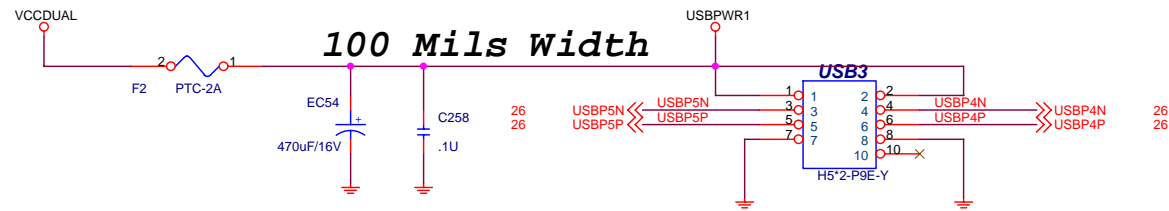


(MCP51 For A02) AE4 , AE3 , AF3 also change to 1.5V_DUAL [20050809]





USB PORT INTERFACE



FGPI1:

High : SMART FAN Support
Low: Not Support

FGPI2:

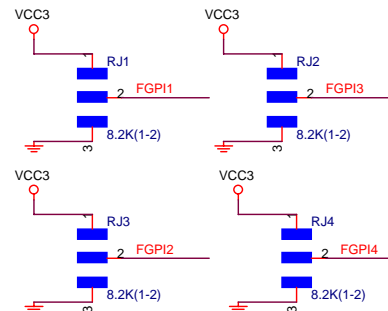
High: Deatect Adjust Voltage
Low: Not Support

FGPI3:

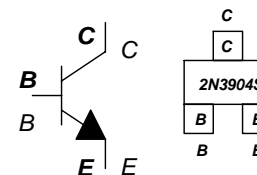
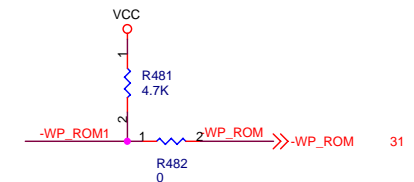
High: STR Support
Low: Not Support

FGPI4:

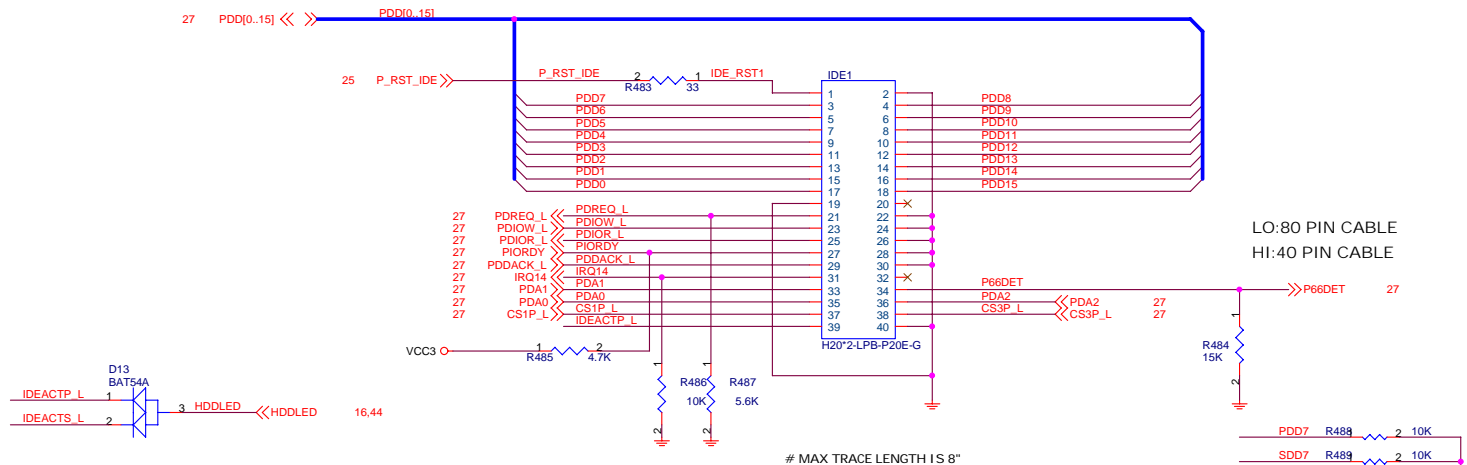
High: Detect COM2
Low: Not Support



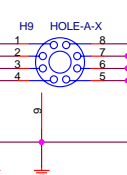
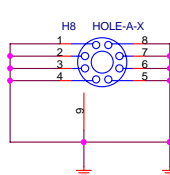
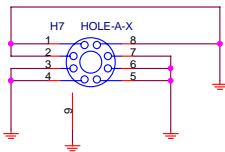
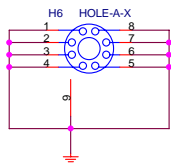
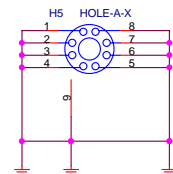
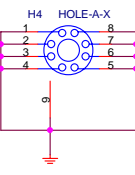
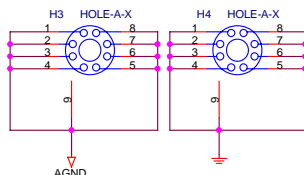
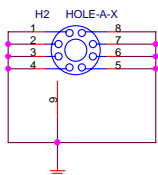
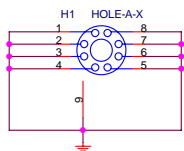
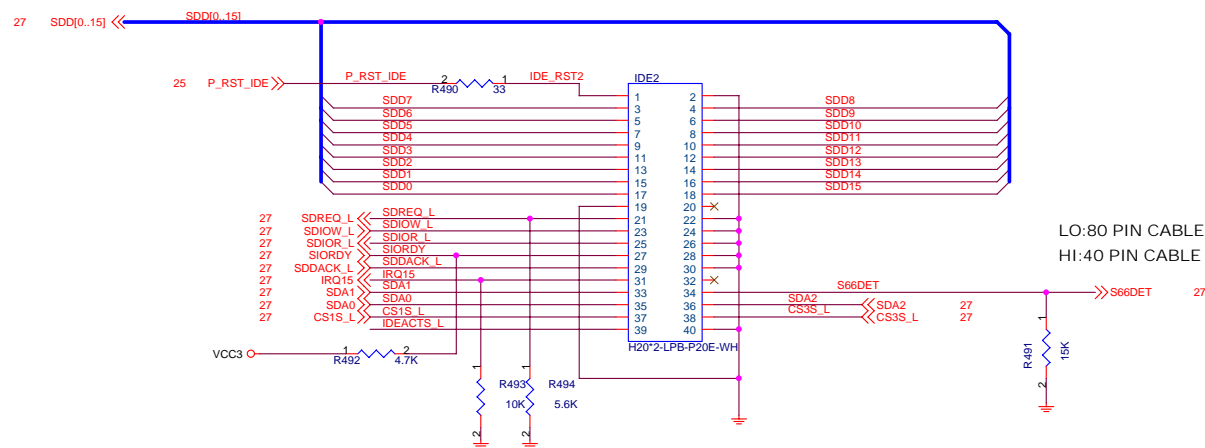
	BIOS PROTECT
1-2	DISABLE
2-3	ENABLE



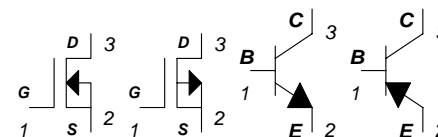
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DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L , XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.



Top View SOT-23



Fan Header

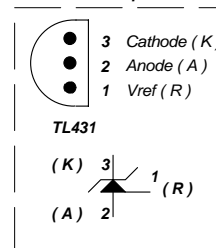


AMP640456-3

TO-263 / TO-252

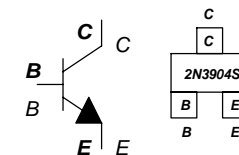
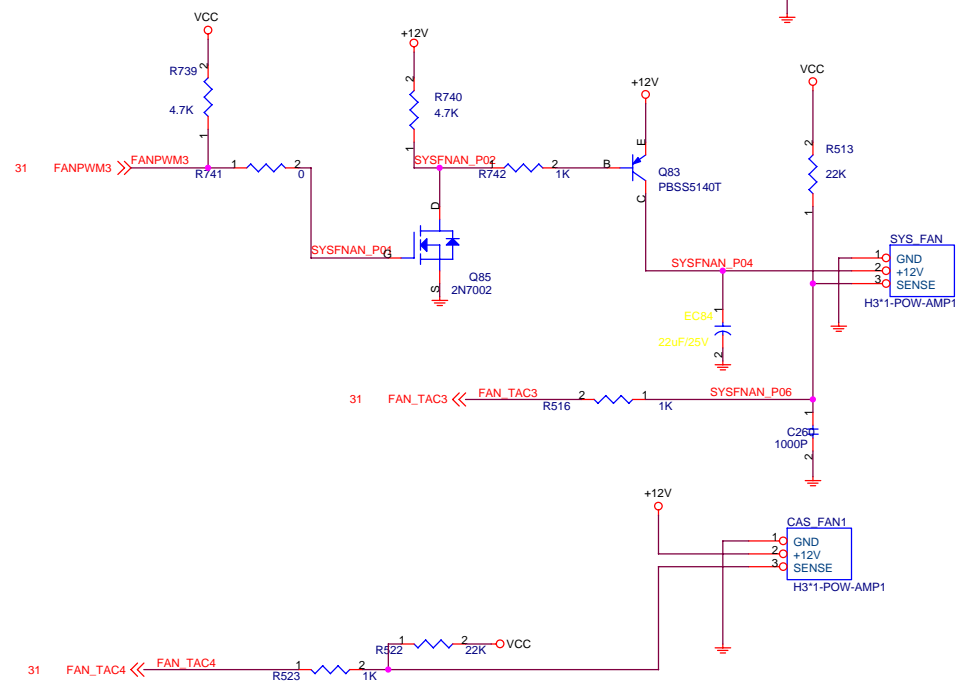
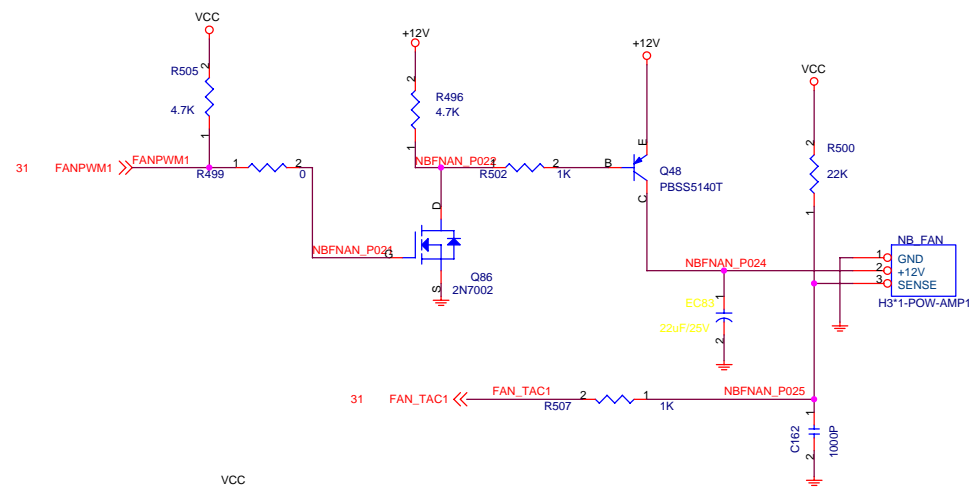


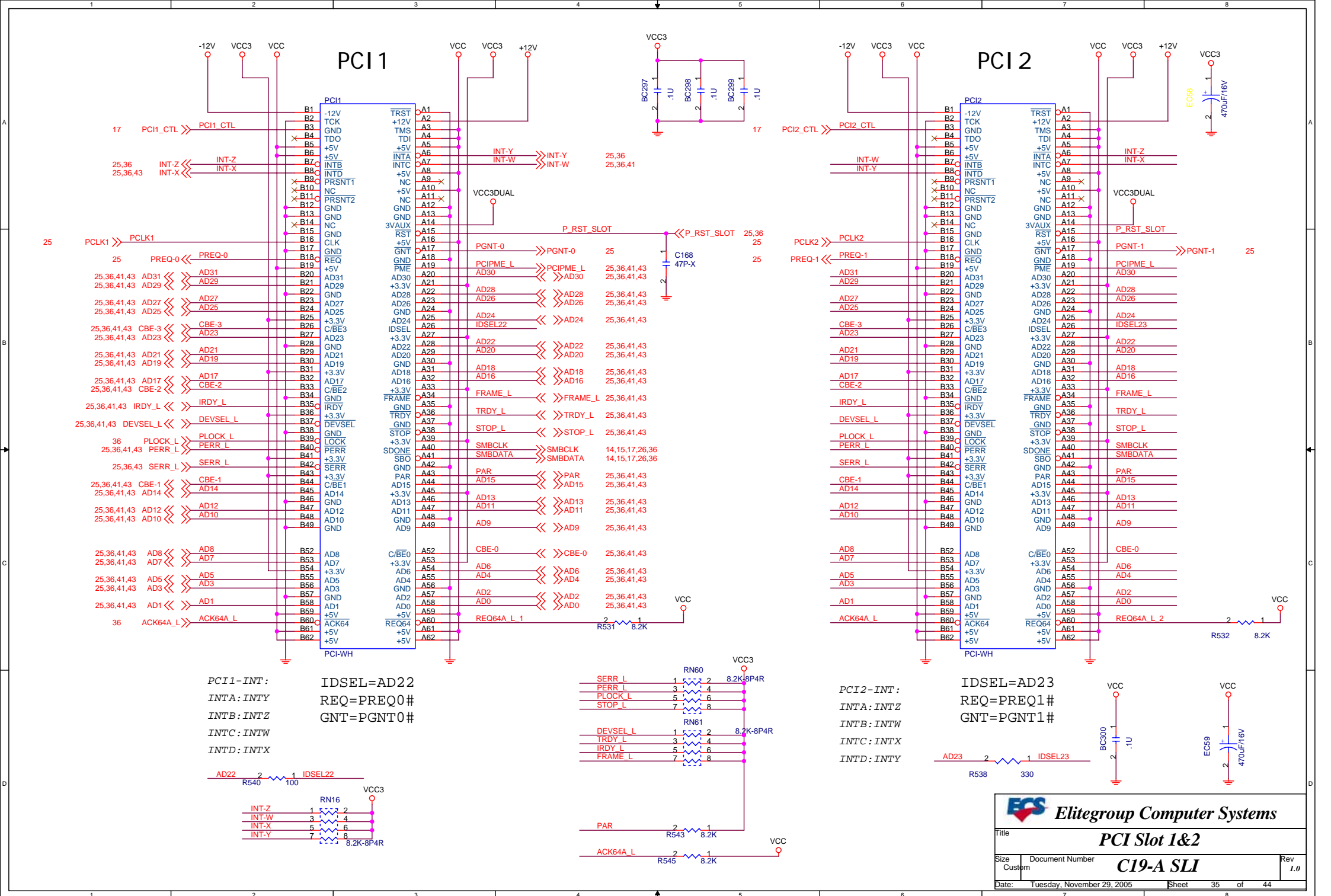
Top View

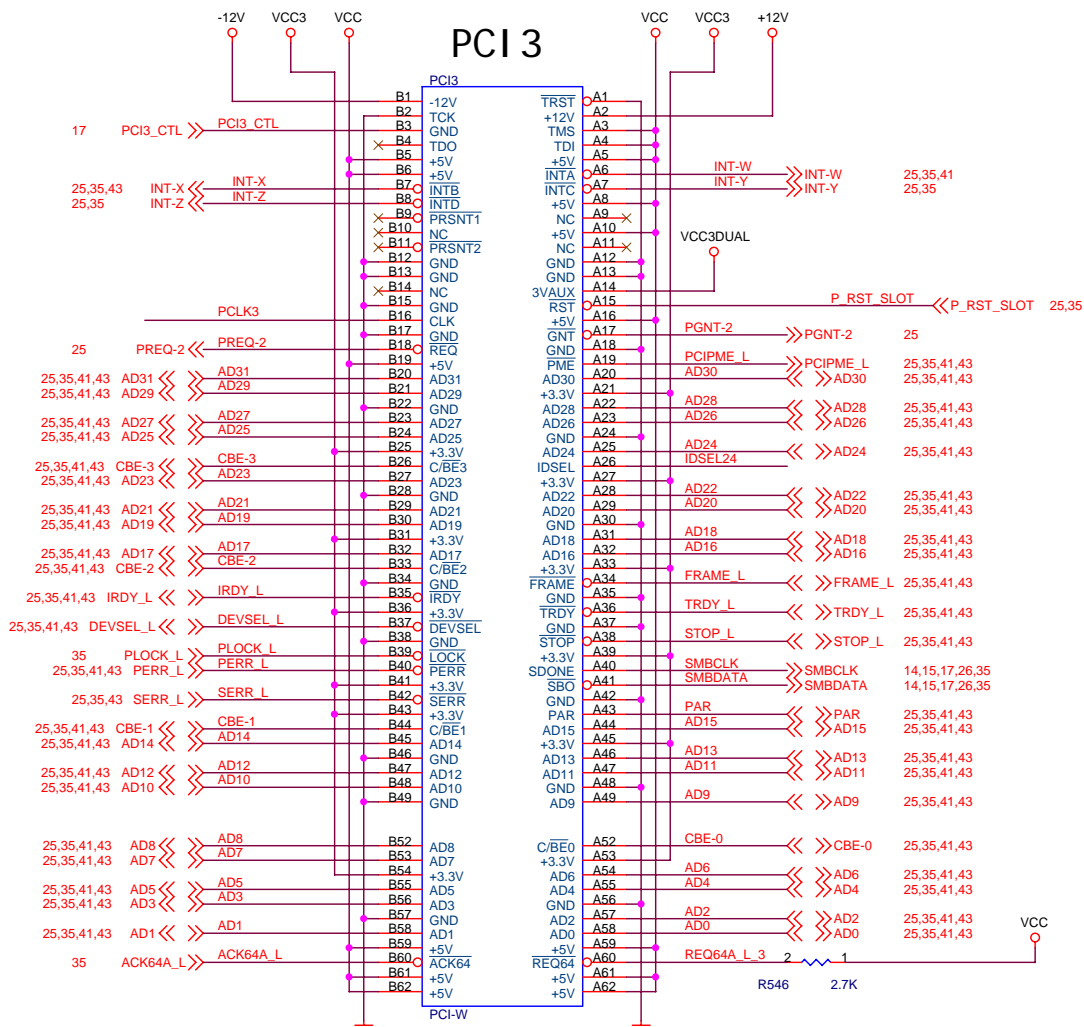


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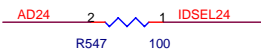
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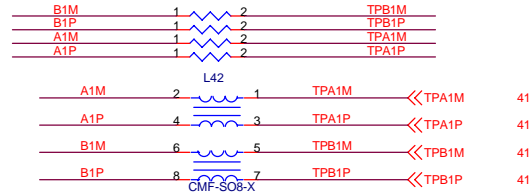
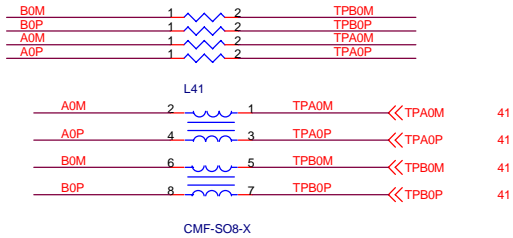




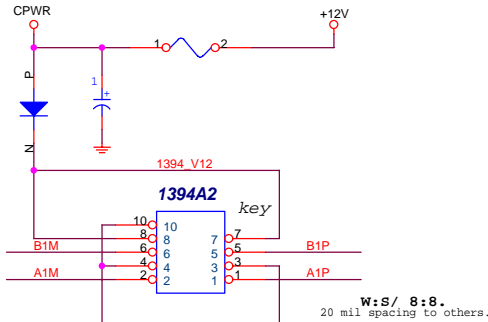
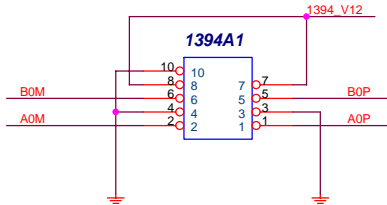
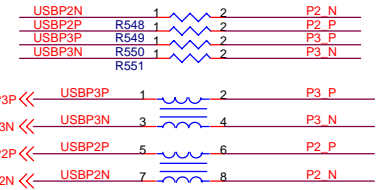


PCI3-INT: IDSEL=AD24
 INTA: INTE REQ=PREQ2#
 INTB: INTF GNT=PGNT2#
 INTC: INTG
 INTD: INTH

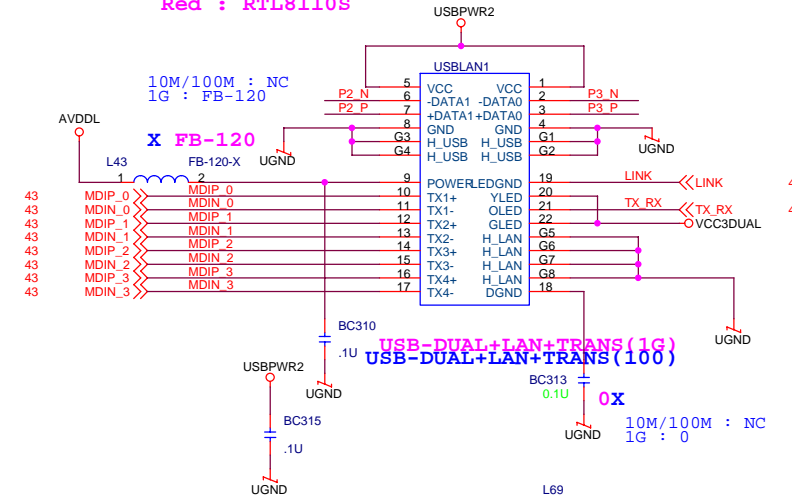




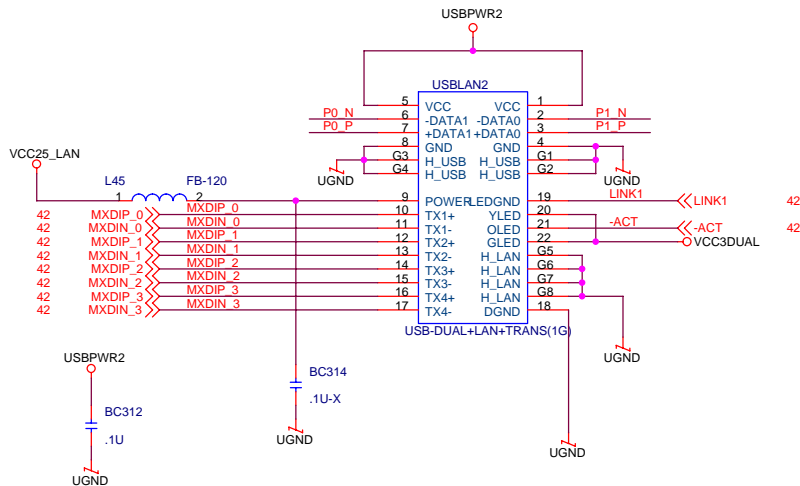
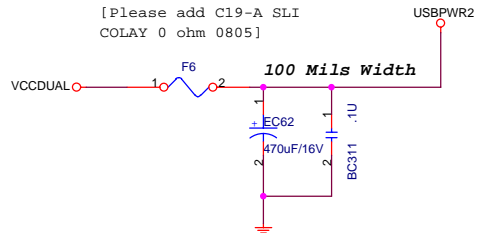
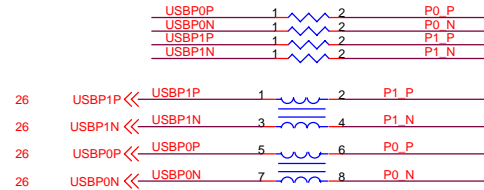
REAR_SIDE

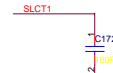
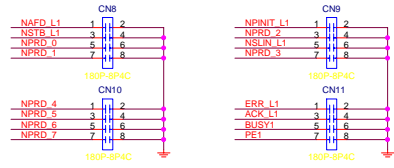
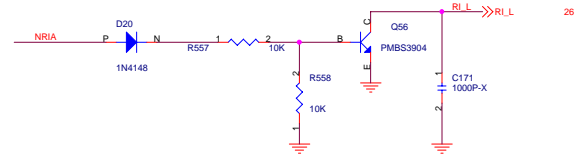
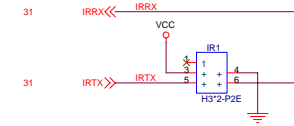


Blue : RTL8100C (Default)
Red : RTL8110S

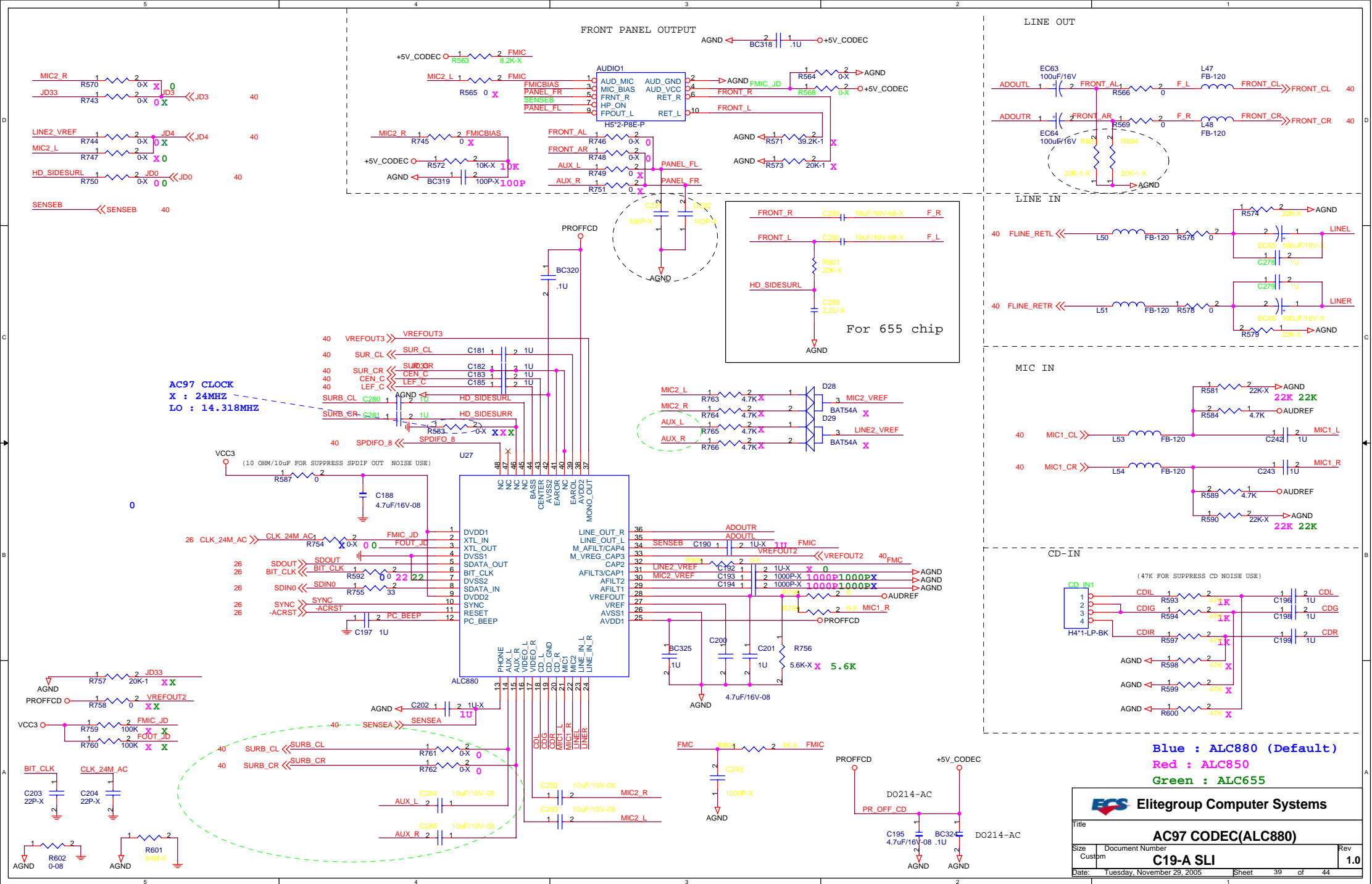


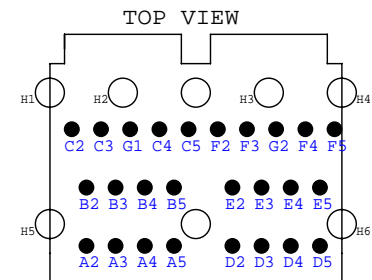
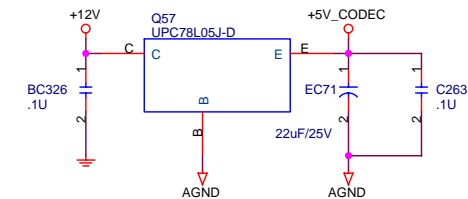
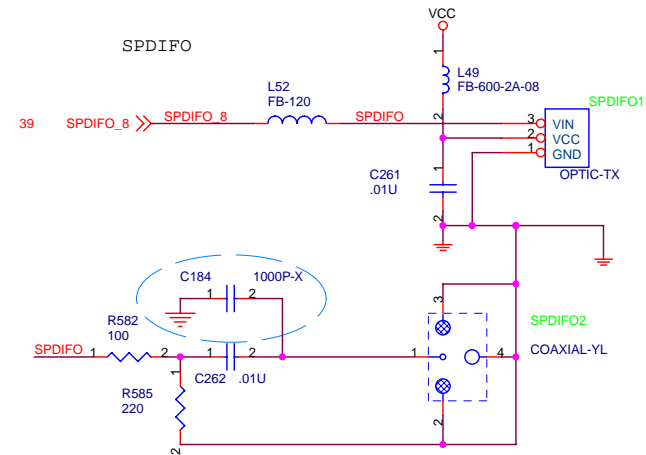
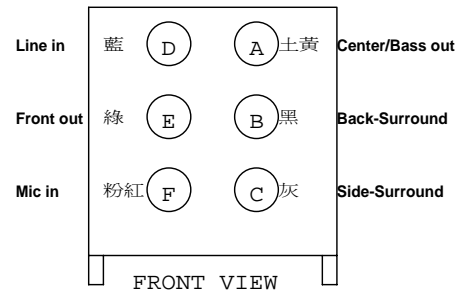
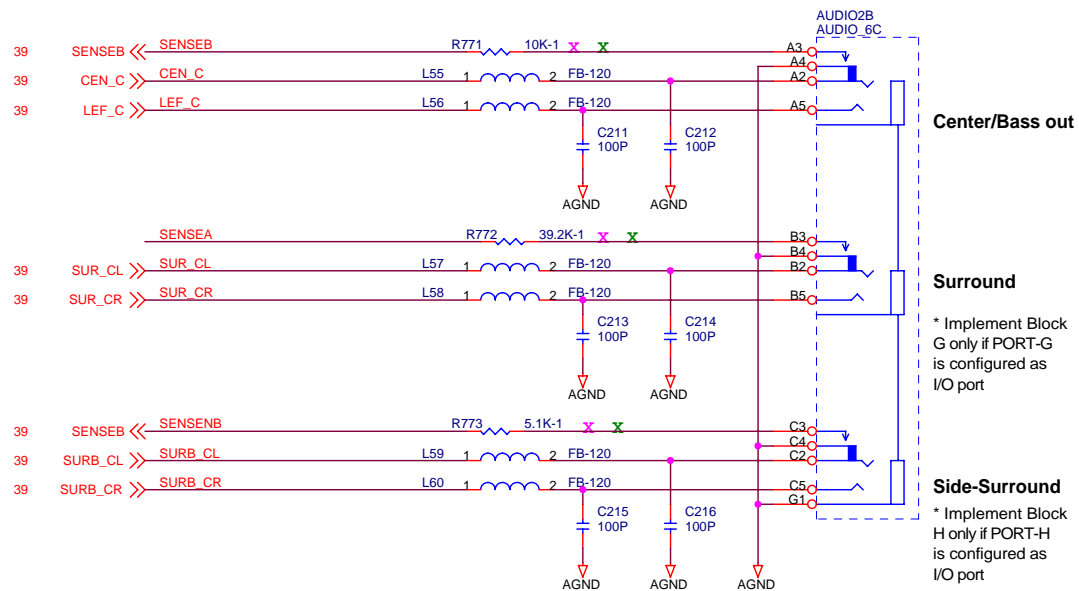
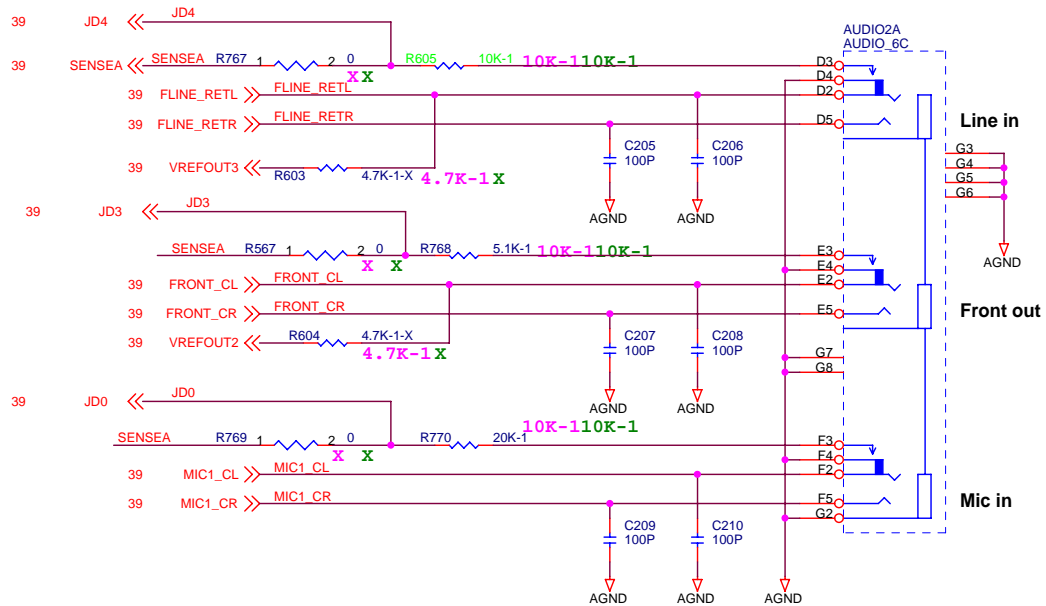
REAR_SIDE

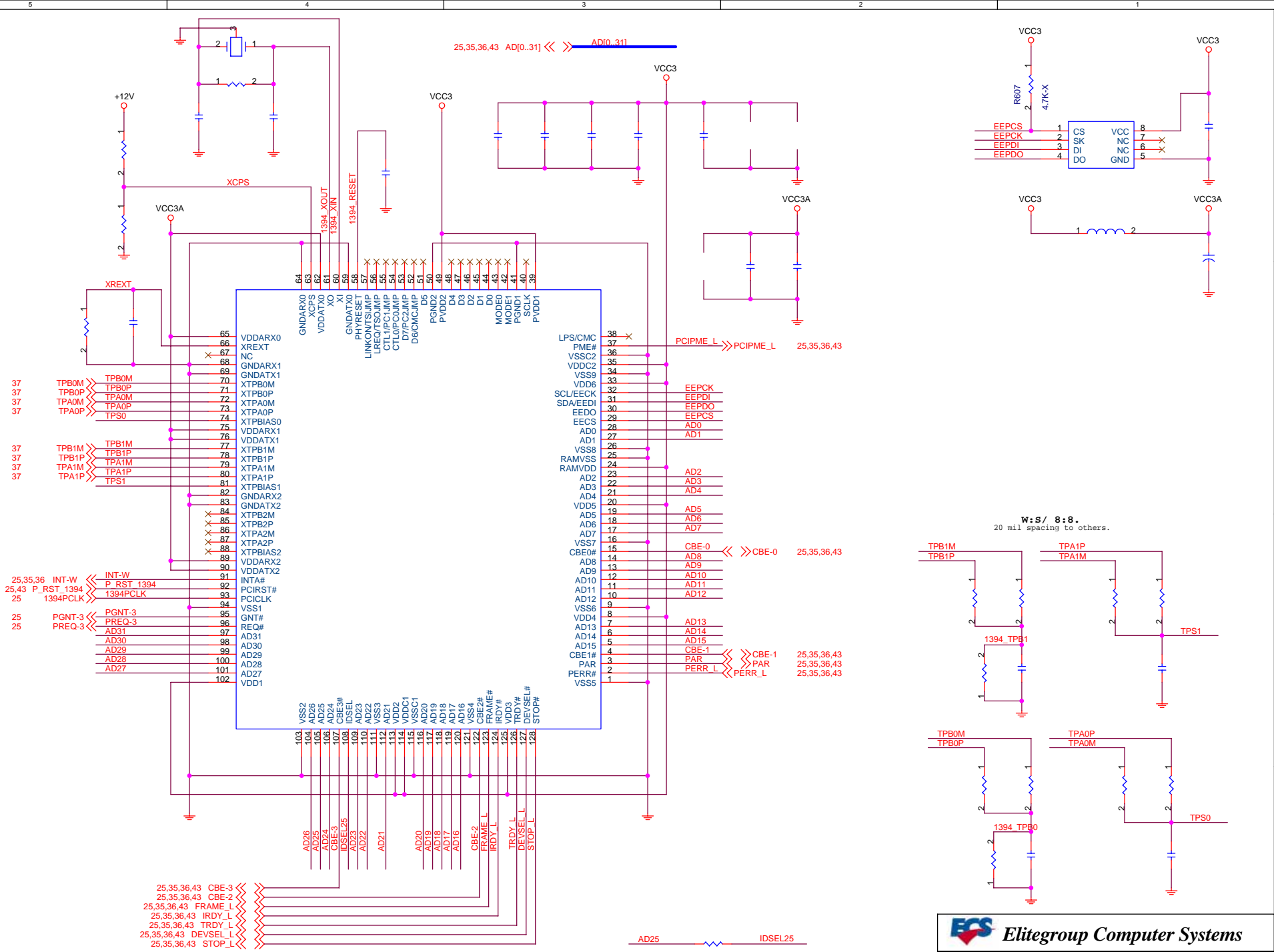





31	PRD3 <L	PRD3	PRD3_1
31	PRD2 <L	PRD2	PRD2_1
31	PRD1 <L	PRD1	PRD1_1
31	PRD0 <L	PRD0	PRD0_1
31	PRD7 <L	PRD7	PRD7_1
31	PRD6 <L	PRD6	PRD6_1
31	PRD5 <L	PRD5	PRD5_1
31	PRD4 <L	PRD4	PRD4_1
31	STB_L <L	STB_L	STB_L1
31	APD_L <L	APD_L	APD_L1
31	ERR <L	ERR_L	ERR_L1
31	PINIT_L <L	PINIT_L	PINIT_L1
31	SUN_L <L	SUN_L	SUN_L1
31	ACK_L <L	ACK_L	ACK_L1
31	BUSY <L	BUSY	BUSY1
31	PE <L	PE	PE1
31	SCT <L	SCT	SCT1







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1.0

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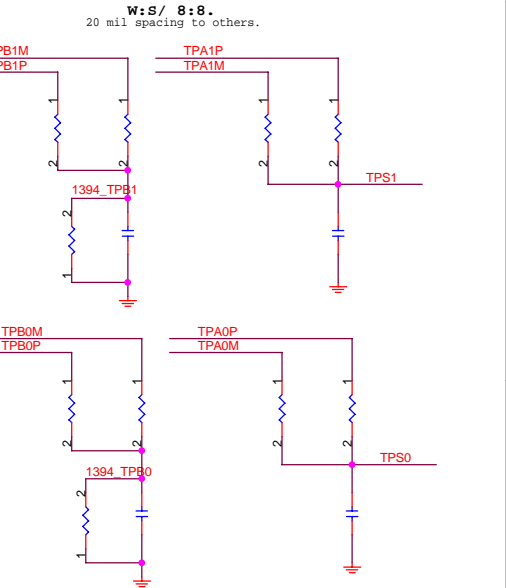
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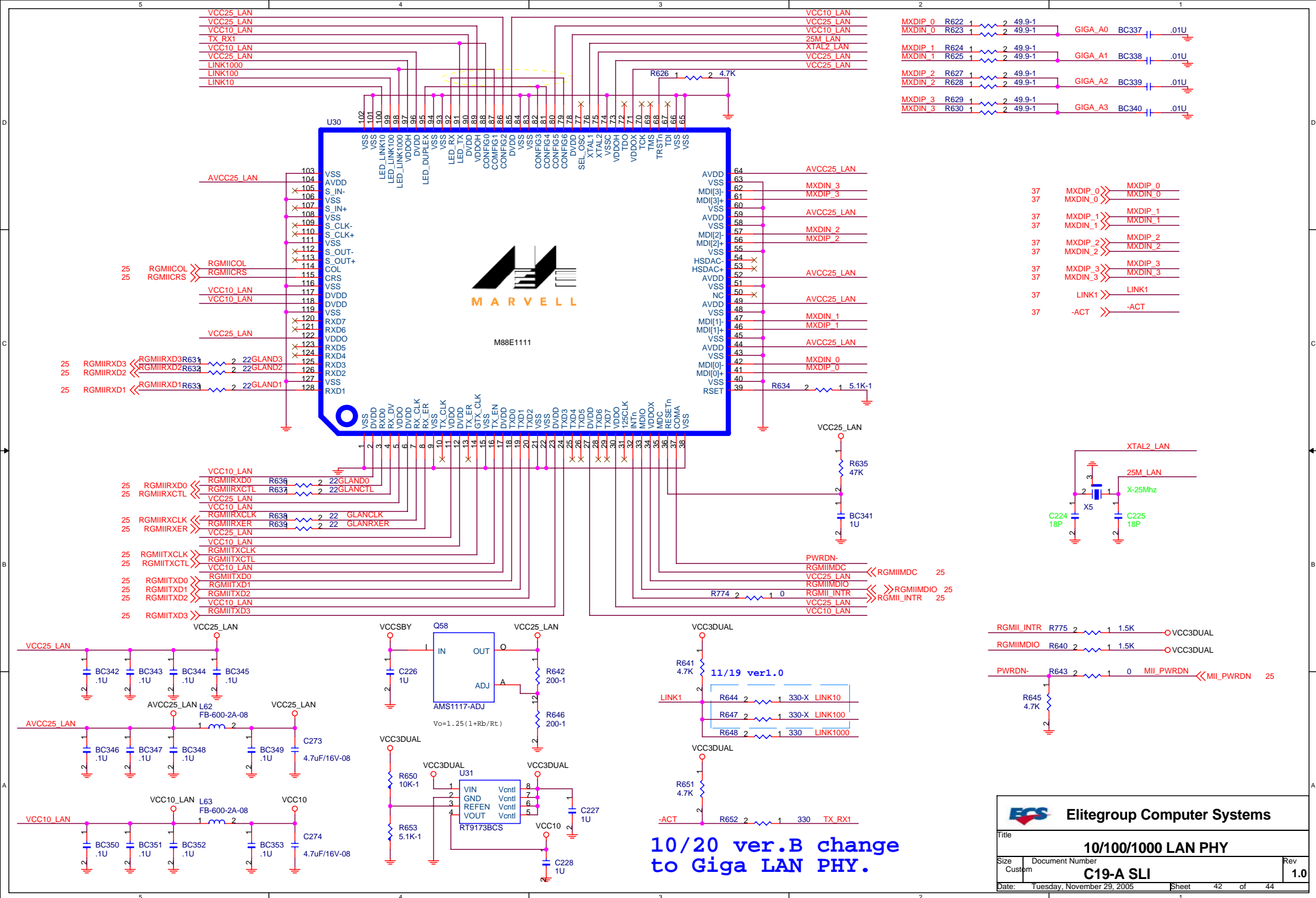
Sheet

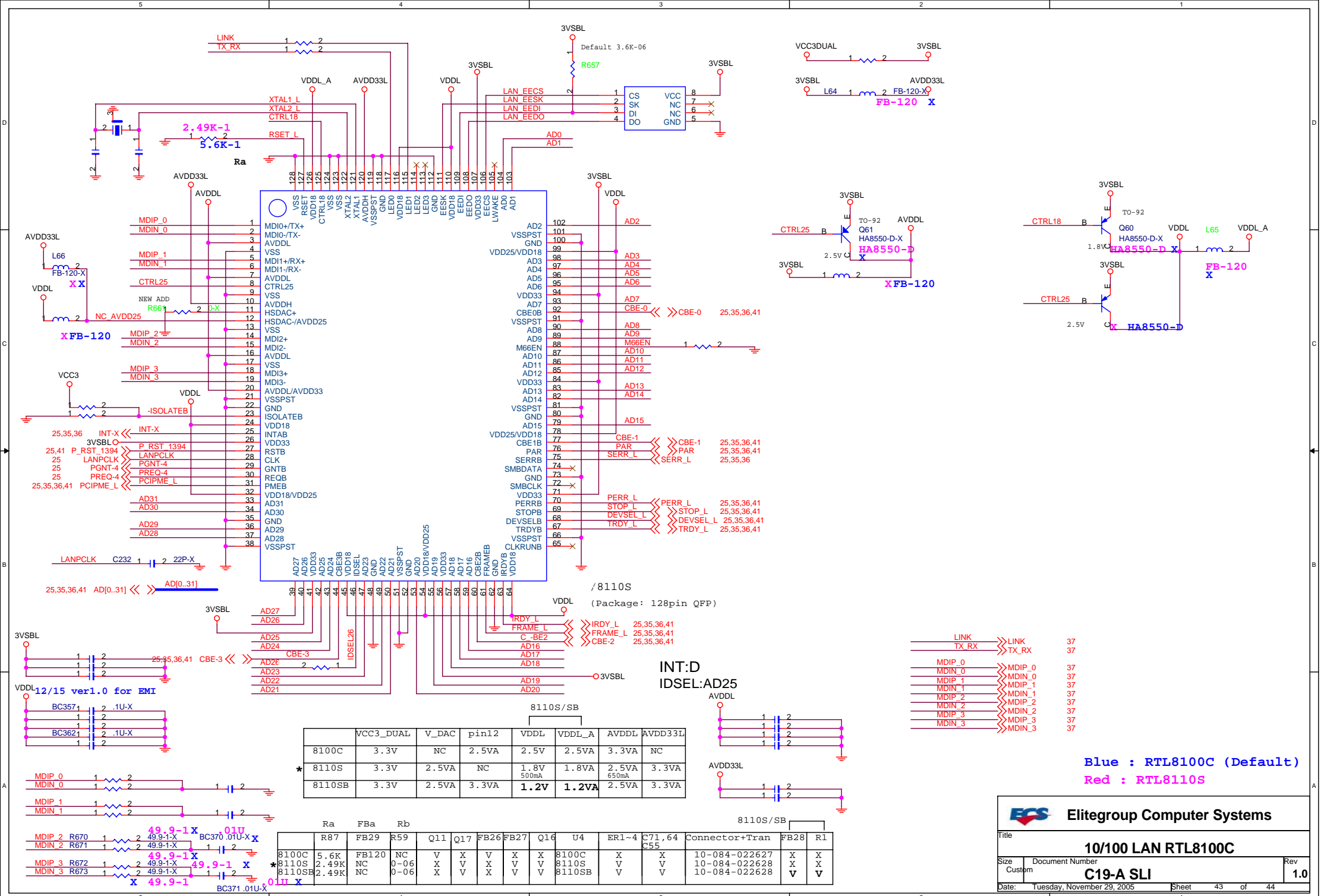
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	VCC3_DUAL	V_DAC	pin12	VDDL	VDDL_A	AVDDL	AVDD33L
8100C	3.3V	NC	2.5VA	2.5V	2.5VA	3.3VA	NC
8110S	3.3V	2.5VA	NC	1.8V 500mA	1.8VA	2.5VA 650mA	3.3VA
8110SB	3.3V	2.5VA	3.3VA	1.2V	1.2VA	2.5VA	3.3VA

	Ra	FBa	Rb	Q11	Q17	FB26	FB27	Q16	U4	ER1~4	C71,64 C55	Connector+Tran	FB28	R1
8100C	5.6K	FB120	NC	V	X	V	X	X	8100C	X	X	10-084-022627	X	X
8110S	2.49K	NC	0-06	X	V	V	V	V	8110S	V	V	10-084-022628	X	X
8110SB	2.49K	NC	0-06	X	V	X	V	V	8110SB	V	V	10-084-022628	V	V

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